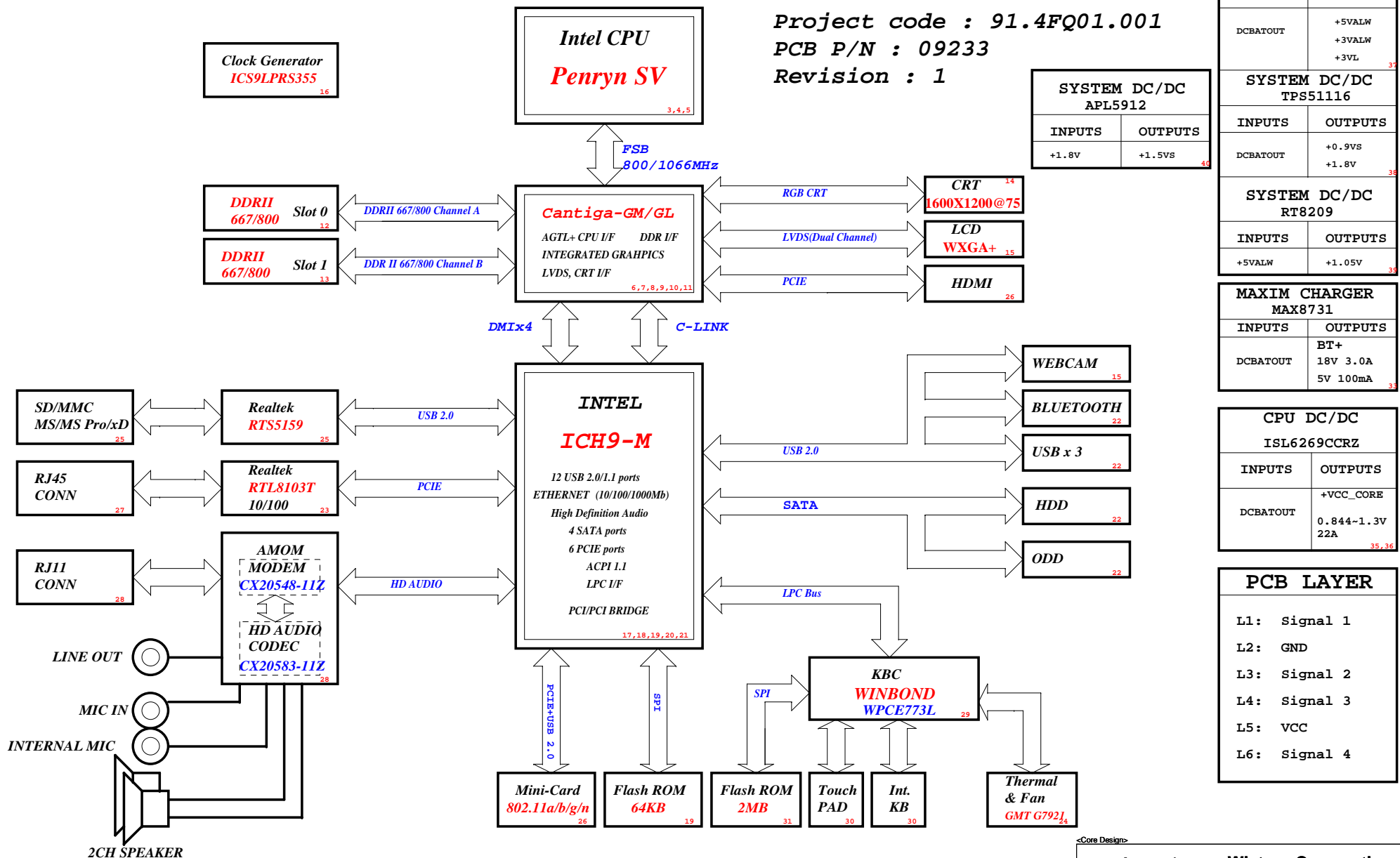


HBU16-1.2 Intel UMA Block Diagram

Project code : 91.4FQ01.001
 PCB P/N : 09233
 Revision : 1



<Core Design>

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size A3 Document Number **HBU16 1.2** Rev **1**

Date: Monday, July 06, 2009 Sheet 1 of 41

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCI Express Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCI Express config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCI Express config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h/bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

PCI Express Routing page 19

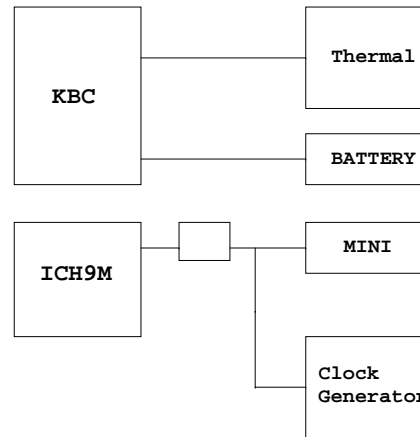
LANE1	LAN
LANE2	MiniCard WLAN

USB Table page 19

Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

SMBus



Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCI Express Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL2 mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

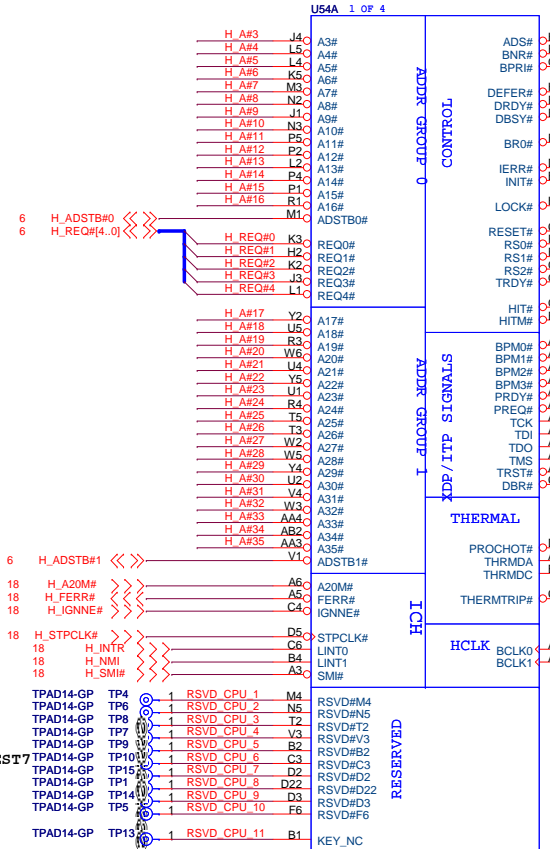
NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

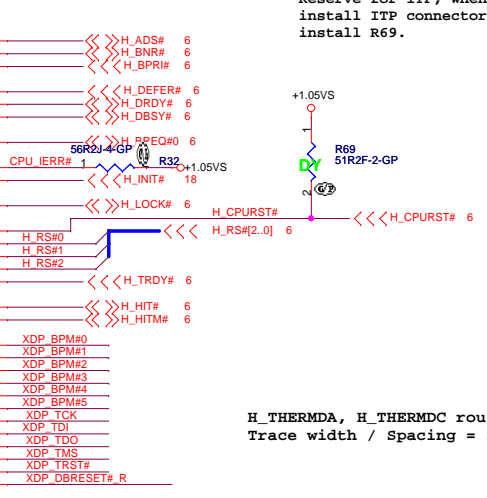
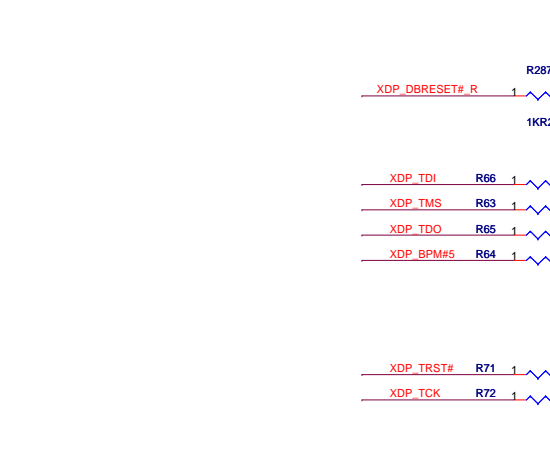
<Core Design>

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Table of Content			
Size A3	Document Number	Rev	
	HBU16 1.2	1	
Date: Tuesday, June 30, 2009	Sheet 2 of 41		

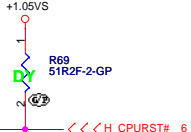
H_A#[35..3] <<< H_A#[35..3]



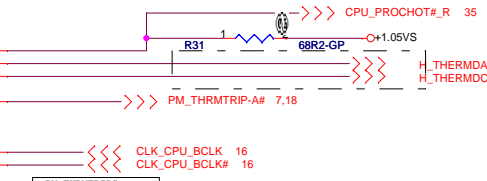
BGA479-SKT6-GPU7
 1st: 62.10079.001
 2nd: 62.10053.401



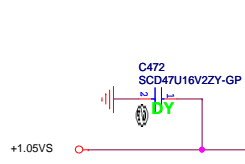
Reserve for ITP, when install ITP connector, install R69.



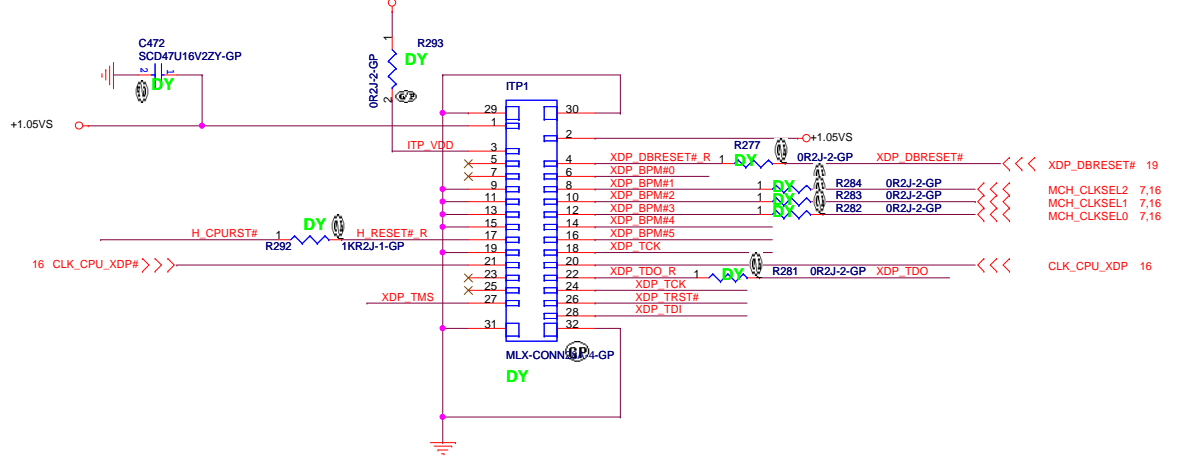
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)



ITP Connector



<Core Design>

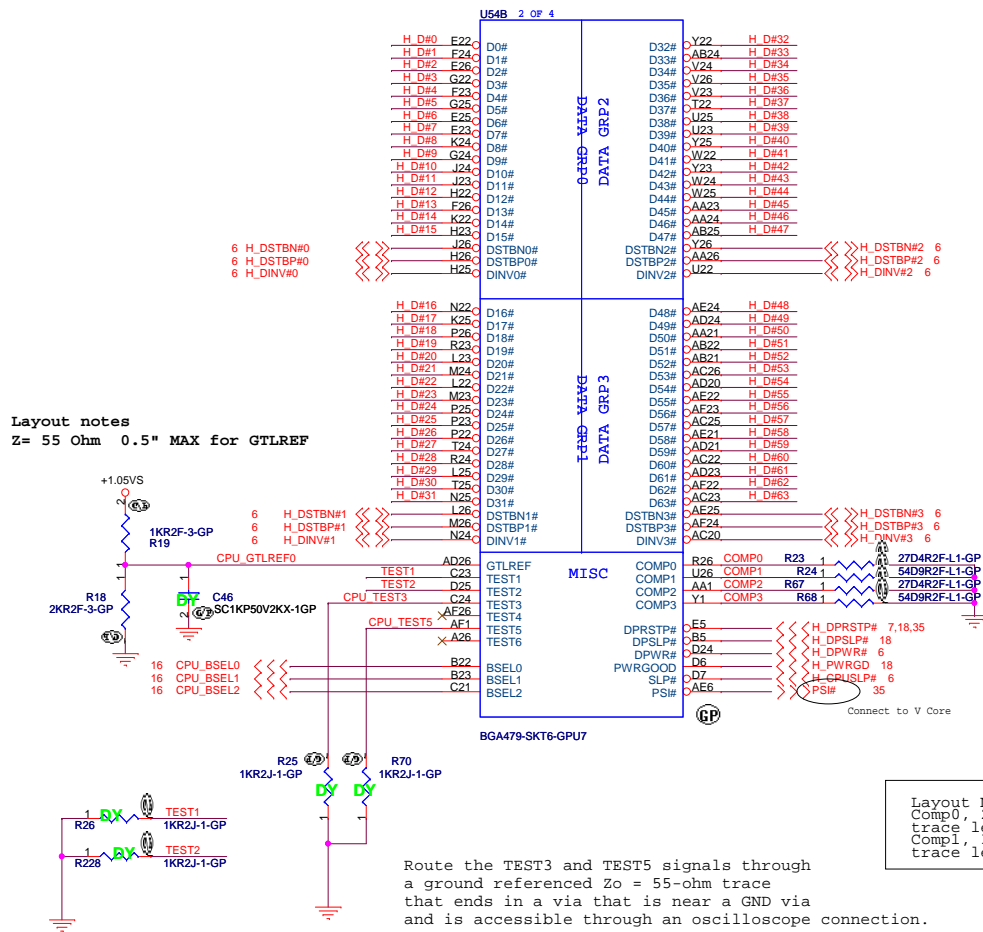
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Title: **CPU (1 of 2)**

Size: Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 3 of 41

H_DINV#[3..0] <<>>H_DINV#[3..0] 6
 H_DSTBN#[3..0] <<>>H_DSTBN#[3..0] 6
 H_DSTBP#[3..0] <<>>H_DSTBP#[3..0] 6
 H_D#[63..0] <<>>H_D#[63..0] 6



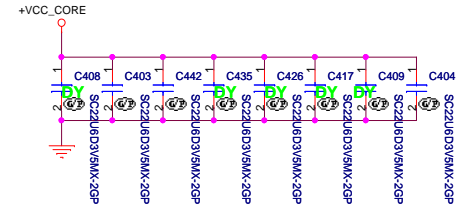
Layout notes
 Z = 55 Ohm 0.5" MAX for GTLREF

Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

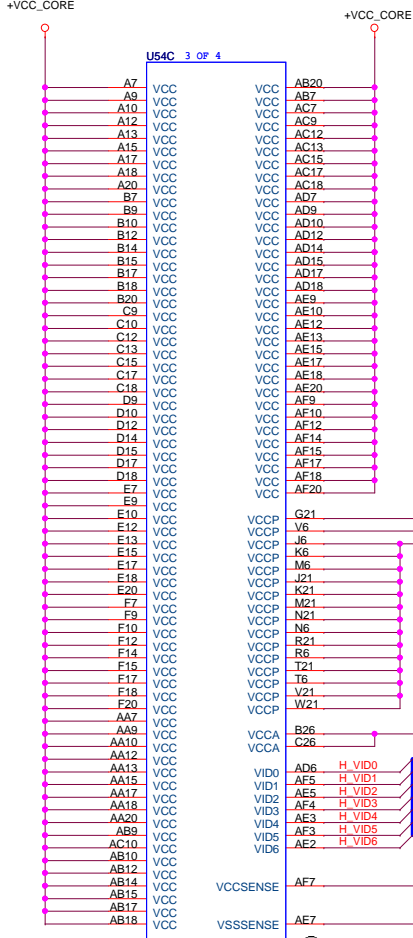
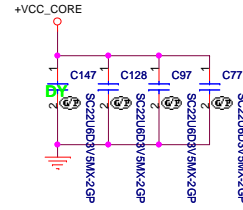
Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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CPU (3 of 2)	
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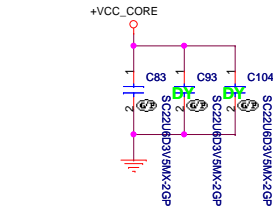
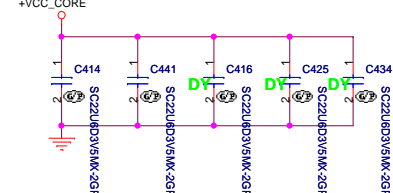
Please these inside socket cavity on L8(North side Secondary)



Please these outside socket cavity on L8(North side Secondary)

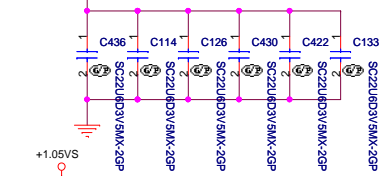


Please these inside socket cavity on L8(South side Secondary)

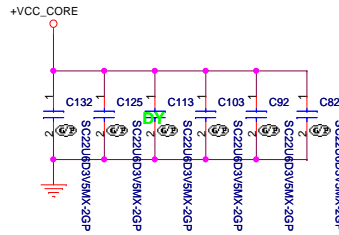


Please these outside socket cavity on L8(South side Secondary)

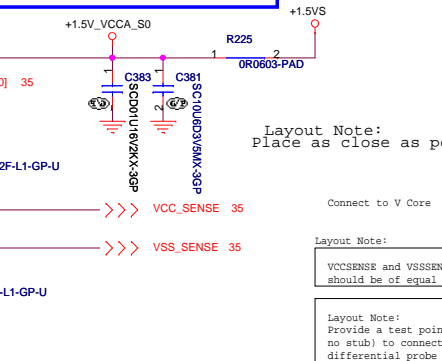
Please these inside socket cavity on L8(North side Primary)



Please these inside socket cavity on L8(South side Primary)



layout note: "1D5V_VCCA_S0" as short as possible

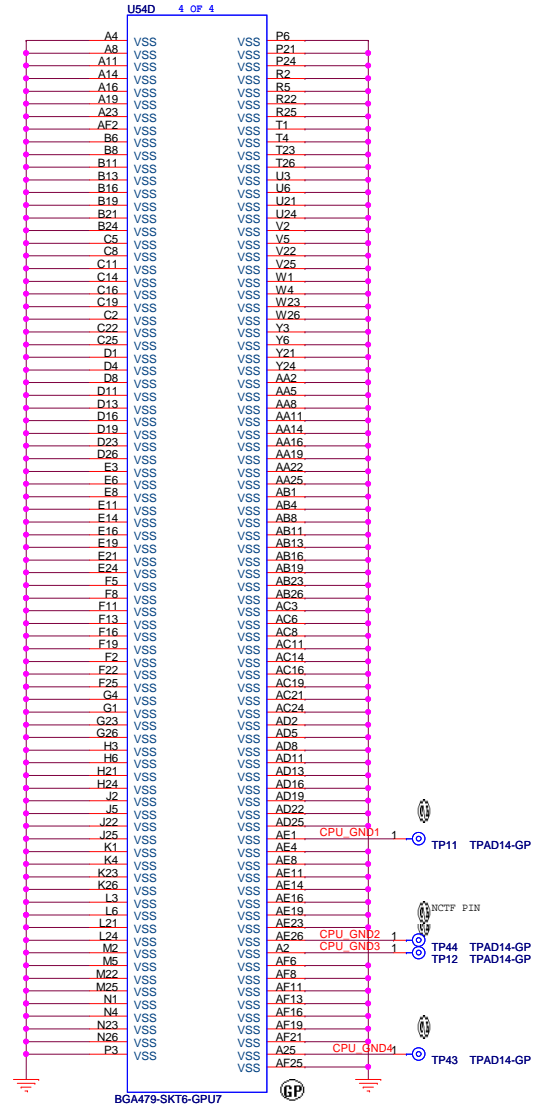
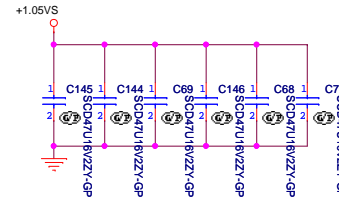


Layout Note: Place as close as possible to the CPU VCCA pin.

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)

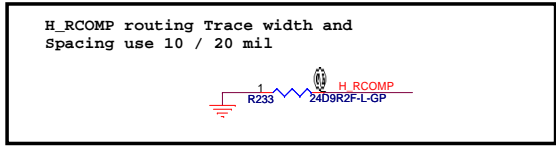
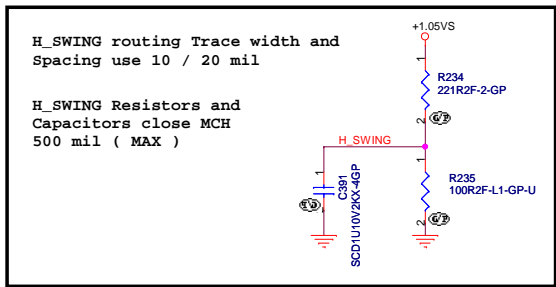


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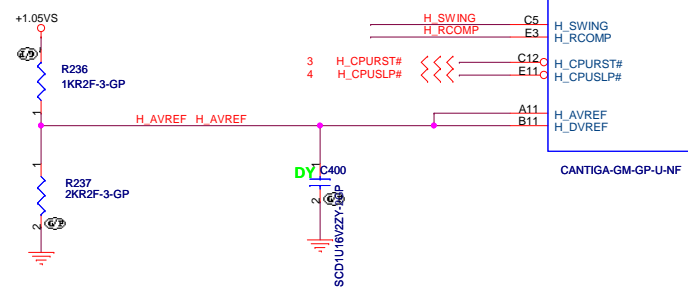
Title: **CPU (3 of 3)**

Size: Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 5 of 41



Place them near to the chip (< 0.5")



U53A 1 of 10

H_D#0	F2	H_D#_0
H_D#1	G8	H_D#_1
H_D#2	FR	H_D#_2
H_D#3	E6	H_D#_3
H_D#4	G2	H_D#_4
H_D#5	H6	H_D#_5
H_D#6	H2	H_D#_6
H_D#7	F6	H_D#_7
H_D#8	D4	H_D#_8
H_D#9	H3	H_D#_9
H_D#10	M9	H_D#_10
H_D#11	M1	H_D#_11
H_D#12	J2	H_D#_12
H_D#13	J2	H_D#_13
H_D#14	N12	H_D#_14
H_D#15	J6	H_D#_15
H_D#16	L2	H_D#_16
H_D#17	R2	H_D#_17
H_D#18	R2	H_D#_18
H_D#19	N9	H_D#_19
H_D#20	L8	H_D#_20
H_D#21	M5	H_D#_21
H_D#22	J3	H_D#_22
H_D#23	N2	H_D#_23
H_D#24	R1	H_D#_24
H_D#25	N5	H_D#_25
H_D#26	N6	H_D#_26
H_D#27	P13	H_D#_27
H_D#28	N8	H_D#_28
H_D#29	L7	H_D#_29
H_D#30	N10	H_D#_30
H_D#31	M3	H_D#_31
H_D#32	Y3	H_D#_32
H_D#33	AD14	H_D#_33
H_D#34	Y6	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	Y12	H_D#_36
H_D#37	Y14	H_D#_37
H_D#38	Y7	H_D#_38
H_D#39	V2	H_D#_39
H_D#40	A8	H_D#_40
H_D#41	Y9	H_D#_41
H_D#42	AA13	H_D#_42
H_D#43	AA9	H_D#_43
H_D#44	AA11	H_D#_44
H_D#45	AD11	H_D#_45
H_D#46	AD10	H_D#_46
H_D#47	AD13	H_D#_47
H_D#48	AE12	H_D#_48
H_D#49	AE8	H_D#_49
H_D#50	AA2	H_D#_50
H_D#51	AD8	H_D#_51
H_D#52	AA3	H_D#_52
H_D#53	AD3	H_D#_53
H_D#54	AD7	H_D#_54
H_D#55	AE14	H_D#_55
H_D#56	AE3	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AE3	H_D#_58
H_D#59	AC3	H_D#_59
H_D#60	AE11	H_D#_60
H_D#61	AE8	H_D#_61
H_D#62	AG2	H_D#_62
H_D#63	AD6	H_D#_63

HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	P17	H_A#14
H_A#_15	F17	H_A#15
H_A#_16	G20	H_A#16
H_A#_17	B19	H_A#17
H_A#_18	J16	H_A#18
H_A#_19	E20	H_A#19
H_A#_20	H16	H_A#20
H_A#_21	J20	H_A#21
H_A#_22	L17	H_A#22
H_A#_23	A17	H_A#23
H_A#_24	B17	H_A#24
H_A#_25	L16	H_A#25
H_A#_26	C21	H_A#26
H_A#_27	J17	H_A#27
H_A#_28	H20	H_A#28
H_A#_29	B18	H_A#29
H_A#_30	K17	H_A#30
H_A#_31	B20	H_A#31
H_A#_32	F21	H_A#32
H_A#_33	K21	H_A#33
H_A#_34	L20	H_A#34
H_A#_35	L20	H_A#35

H_ADSP#	CH12	H_ADSP# 3
H_ADSTB#_0	B16	H_ADSTB# 3
H_ADSTB#_1	G17	H_ADSTB#1 3
H_BNR#	A9	H_BNR# 3
H_BPR#	E11	H_BPR# 3
H_BREQ#	G12	H_BREQ# 3
H_DEFER#	E3	H_DEFER# 3
H_DBSY#	B10	H_DBSY# 3
HPLL_CLK#	AH7	CLK_MCH_BCLK# 16
HPLL_CLK#	AH6	CLK_MCH_BCLK# 16
H_DPWR#	J11	H_DPWR# 4
H_DRDY#	C9	H_DRDY# 3
H_HIT#	E12	H_HIT# 3
H_LOCK#	CH11	H_LOCK# 3
H_TRDY#	C9	H_TRDY# 3

H_DINV#_0	J8	H_DINV#0
H_DINV#_1	L3	H_DINV#1
H_DINV#_2	Y13	H_DINV#2
H_DINV#_3	Y1	H_DINV#3

H_DSTBN#_0	L10	H_DSTBN#0
H_DSTBN#_1	AA5	H_DSTBN#1
H_DSTBN#_2	AE6	H_DSTBN#2
H_DSTBN#_3	AE6	H_DSTBN#3

H_DSTBP#_0	L9	H_DSTBP#0
H_DSTBP#_1	M6	H_DSTBP#1
H_DSTBP#_2	AA6	H_DSTBP#2
H_DSTBP#_3	AE5	H_DSTBP#3

H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	F13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4

H_RS#_0	B6	H_RS#0
H_RS#_1	F12	H_RS#1
H_RS#_2	C8	H_RS#2

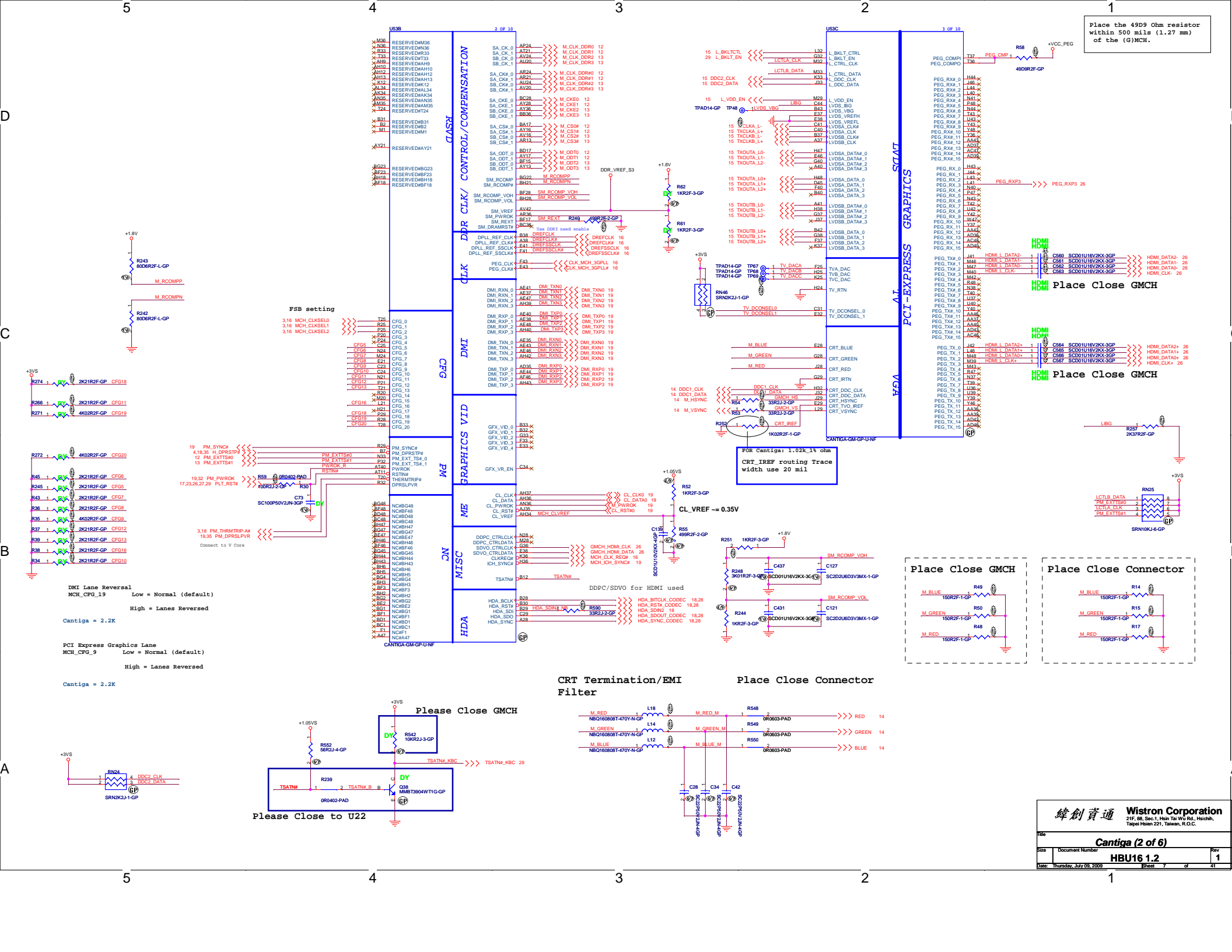
<Core Design>

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Title: **Contiga (1 of 6)**

Size: Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 6 of 41



Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

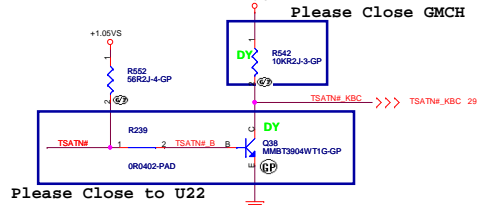
C

B

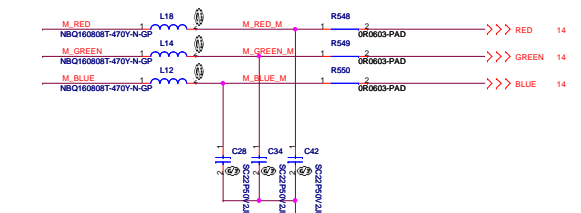
A

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

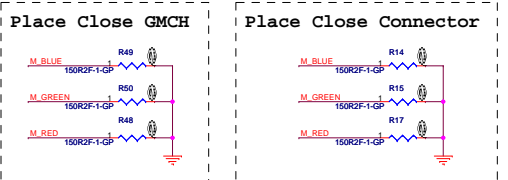
PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K



CRT Termination/EMI Filter

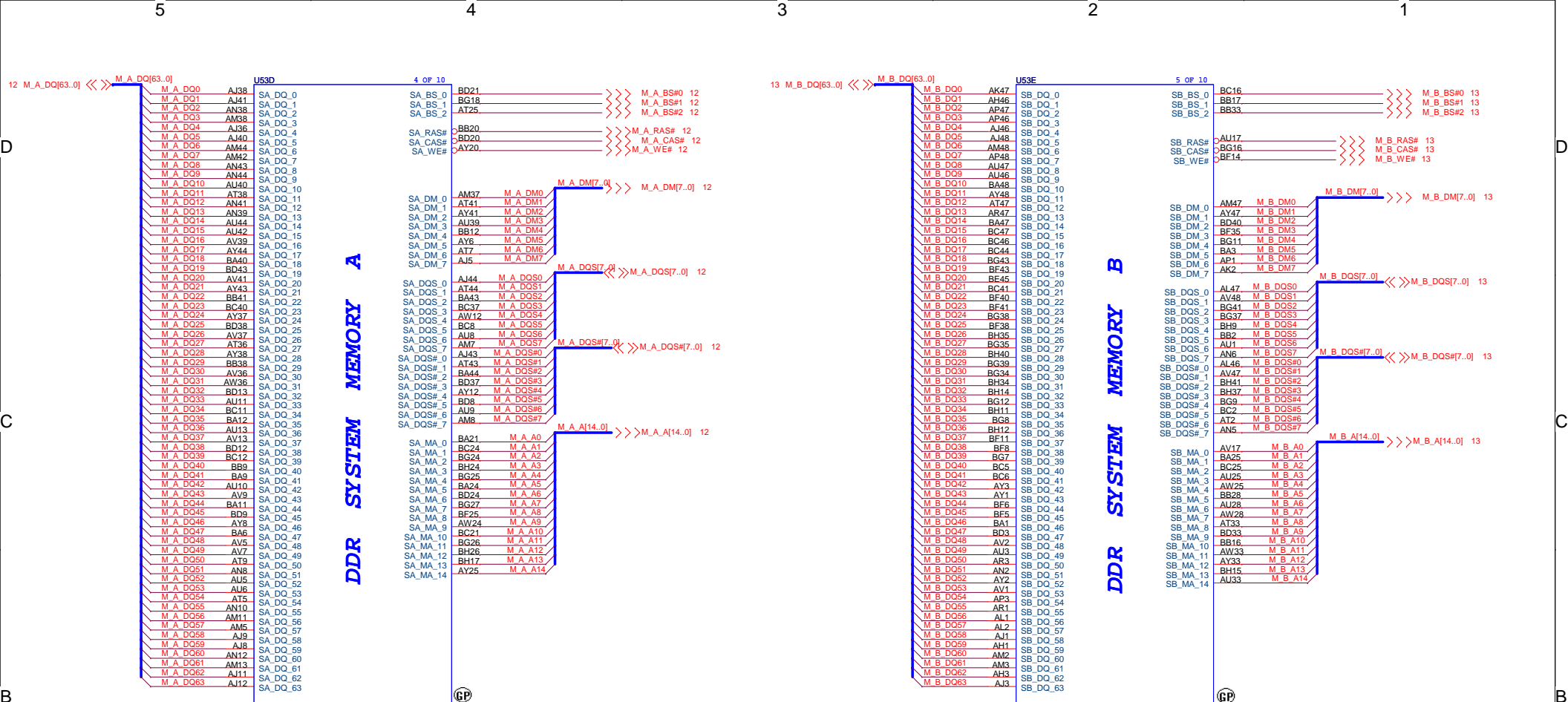


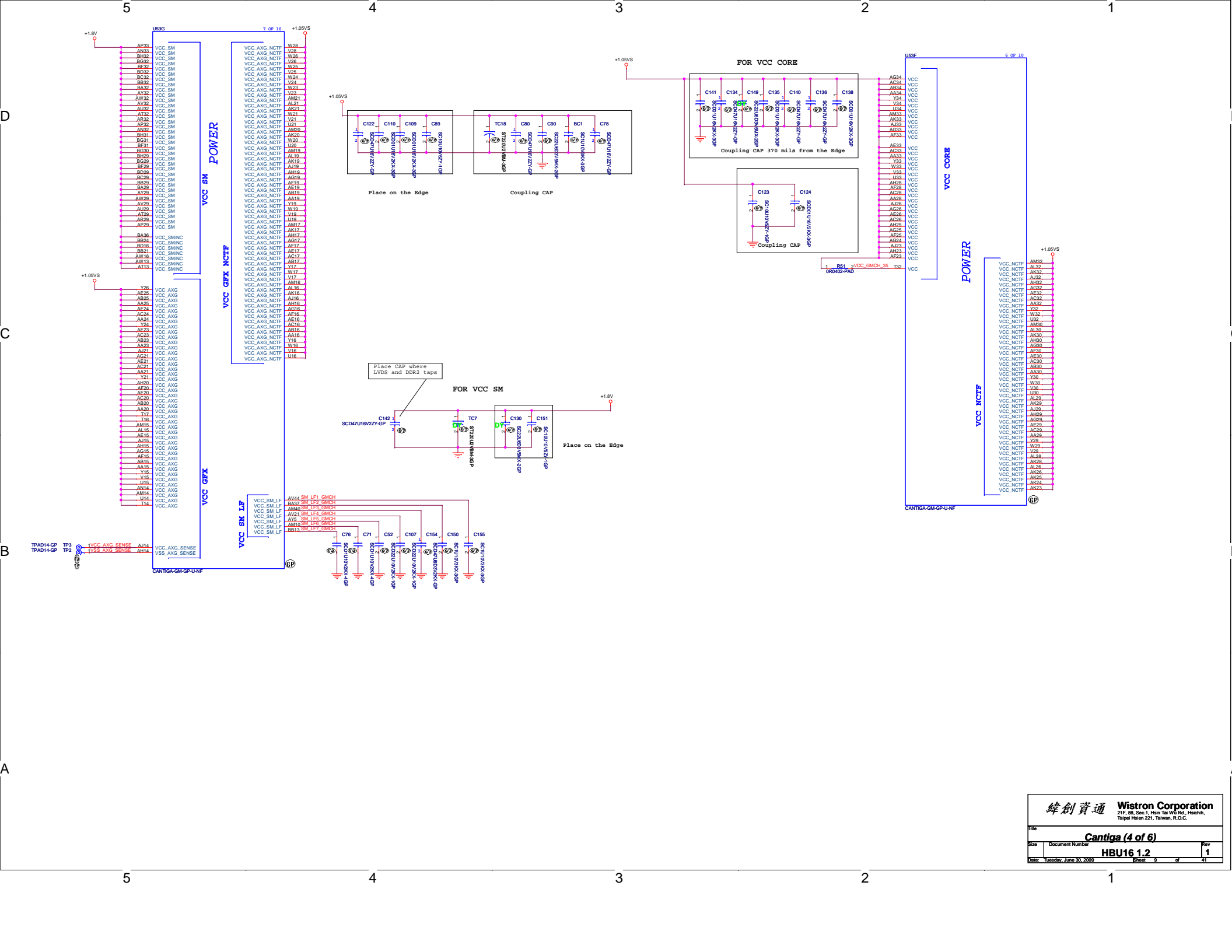
Place Close Connector Filter

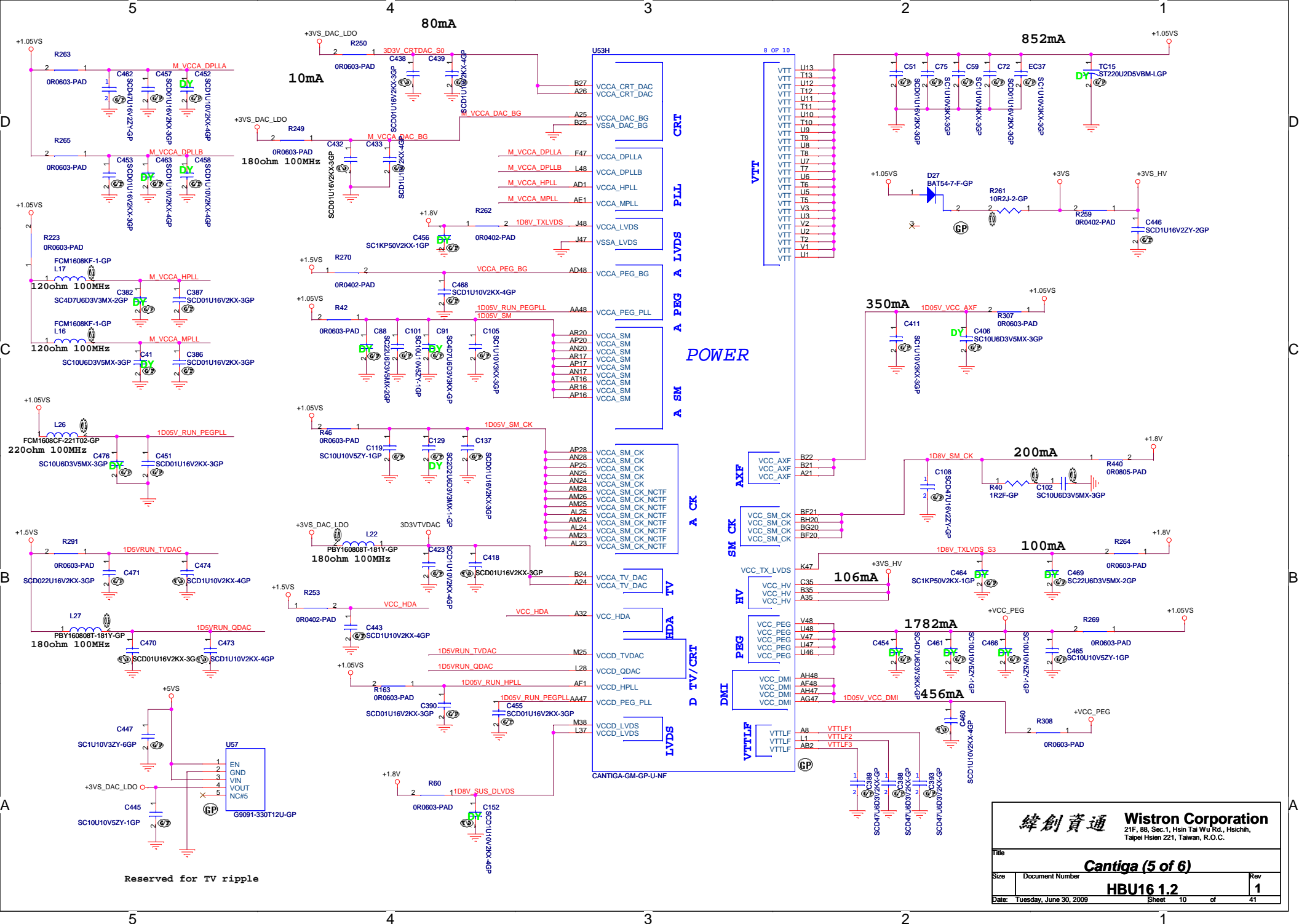


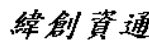
緯創資通 Wistron Corporation
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

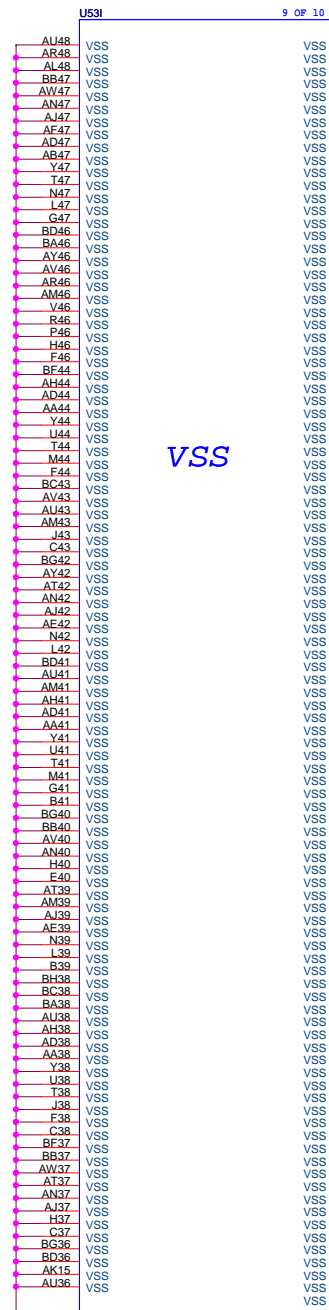
<p>Cantiga (2 of 6)</p>		
Doc No:	HBU16.2	Rev: 1
Date:	Thursday, July 09, 2009	Sheet 7 of 41







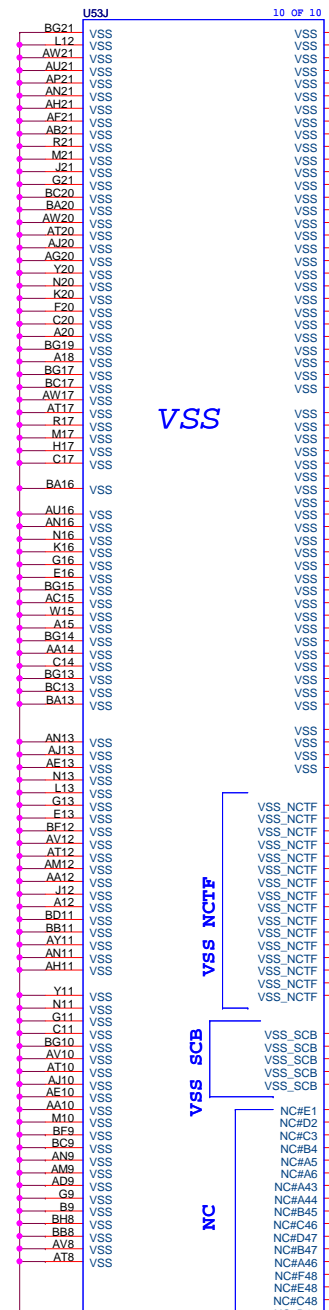
 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Cantiga (5 of 6)	
Title:	Rev: 1
Size:	Document Number: HBU16.1.2
Date: Tuesday, June 30, 2009	Sheet: 10 of 41



CANTIGA-GM-GP-U-NF

Modification AJ6 to reserved Pin

OR0402-PAD

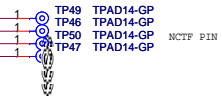
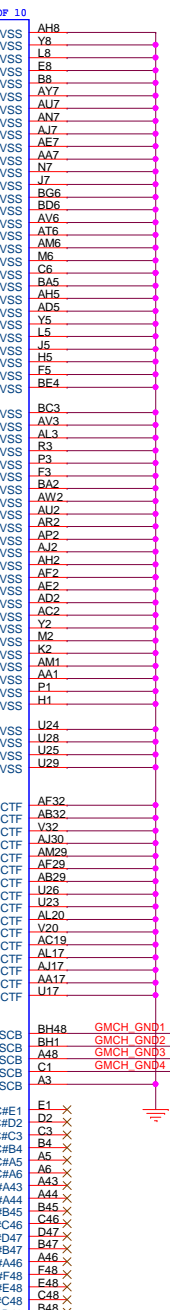


VSS

VSS NCTF

VSS SCB

NC



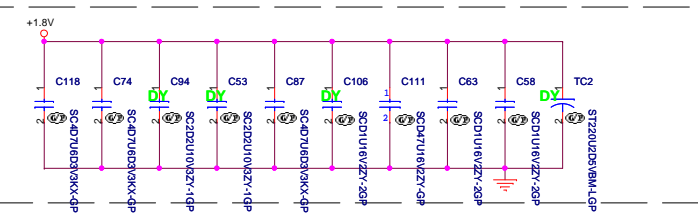
緯創資通 Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

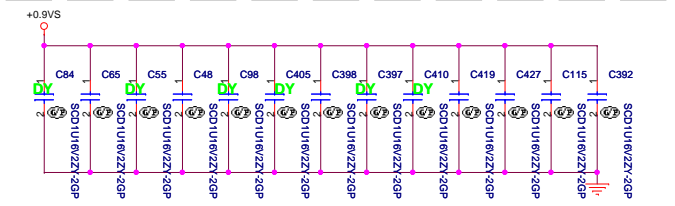
Title			Cantiga (6 of 6)		
Size	Document Number				Rev
HBU16 1.2					1
Date:	Tuesday, June 30, 2009	Sheet	11	of	41

8 M_A_DQS#[7..0] <<<<
 8 M_A_DQ[63..0] <<<<
 8 M_A_DM[7..0] <<<<
 8 M_A_DQS#[7..0] <<<<
 8 M_A_A[14..0] <<<<

Layout Note:
Place near DM1



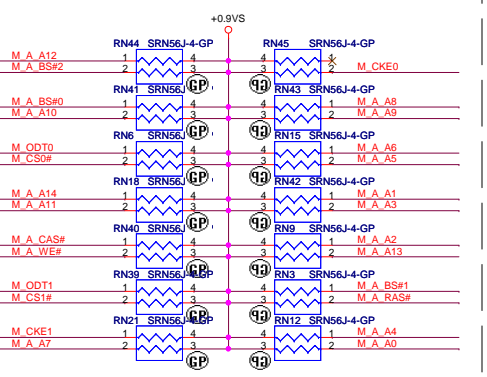
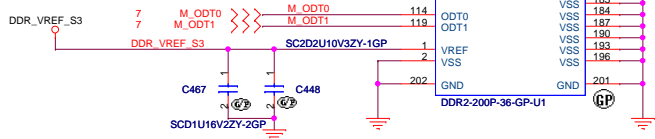
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



8 M_A_BS#2 >>>>
 8 M_A_BS#0 >>>>
 8 M_A_BS#1 >>>>

M_A A0	102	A0
M_A A1	101	A1
M_A A2	100	A2
M_A A3	99	A3
M_A A4	98	A4
M_A A5	97	A5
M_A A6	96	A6
M_A A7	95	A7
M_A A8	94	A8
M_A A9	93	A9
M_A A10	92	A10
M_A A11	91	A11
M_A A12	90	A12
M_A A13	89	A13
M_A A14	88	A14
M_A A15	87	A15
M_A BS#0	107	BA0
M_A BS#1	106	BA1
M_A DQ0	5	DO0
M_A DQ1	7	DO1
M_A DQ2	8	DO2
M_A DQ3	17	DO3
M_A DQ4	19	DO4
M_A DQ5	4	DO5
M_A DQ6	14	DO6
M_A DQ7	18	DO7
M_A DQ8	23	DO8
M_A DQ9	25	DO9
M_A DQ10	35	DO10
M_A DQ11	39	DO11
M_A DQ12	20	DO12
M_A DQ13	22	DO13
M_A DQ14	24	DO14
M_A DQ15	38	DO15
M_A DQ16	43	DO16
M_A DQ17	45	DO17
M_A DQ18	55	DO18
M_A DQ19	57	DO19
M_A DQ20	44	DO20
M_A DQ21	87	DO21
M_A DQ22	56	DO22
M_A DQ23	58	DO23
M_A DQ24	61	DO24
M_A DQ25	63	DO25
M_A DQ26	73	DO26
M_A DQ27	75	DO27
M_A DQ28	62	DO28
M_A DQ29	64	DO29
M_A DQ30	74	DO30
M_A DQ31	76	DO31
M_A DQ32	123	DO32
M_A DQ33	125	DO33
M_A DQ34	135	DO34
M_A DQ35	137	DO35
M_A DQ36	124	DO36
M_A DQ37	126	DO37
M_A DQ38	134	DO38
M_A DQ39	136	DO39
M_A DQ40	141	DO40
M_A DQ41	143	DO41
M_A DQ42	151	DO42
M_A DQ43	153	DO43
M_A DQ44	140	DO44
M_A DQ45	142	DO45
M_A DQ46	152	DO46
M_A DQ47	154	DO47
M_A DQ48	157	DO48
M_A DQ49	159	DO49
M_A DQ50	173	DO50
M_A DQ51	175	DO51
M_A DQ52	158	DO52
M_A DQ53	160	DO53
M_A DQ54	174	DO54
M_A DQ55	176	DO55
M_A DQ56	179	DO56
M_A DQ57	181	DO57
M_A DQ58	189	DO58
M_A DQ59	191	DO59
M_A DQ60	180	DO60
M_A DQ61	182	DO61
M_A DQ62	192	DO62
M_A DQ63	194	DO63

M_A DQS#0	11	/DOS0
M_A DQS#1	29	/DOS1
M_A DQS#2	49	/DOS2
M_A DQS#3	68	/DOS3
M_A DQS#4	129	/DOS4
M_A DQS#5	146	/DOS5
M_A DQS#6	167	/DOS6
M_A DQS#7	186	/DOS7
M_A DQS#0	13	DO50
M_A DQS#1	31	DO51
M_A DQS#2	51	DO52
M_A DQS#3	70	DO53
M_A DQS#4	131	DO54
M_A DQS#5	148	DO55
M_A DQS#6	169	DO56
M_A DQS#7	188	DO57
M_ODT0	114	ODT0
M_ODT1	119	ODT1
VREF	1	VREF
VSS	2	VSS
GND	202	GND



Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"

DM2
 1st: 62.10017.E11
 2nd: 62.10017.691
 3rd: 62.10017.891

<Core Design>

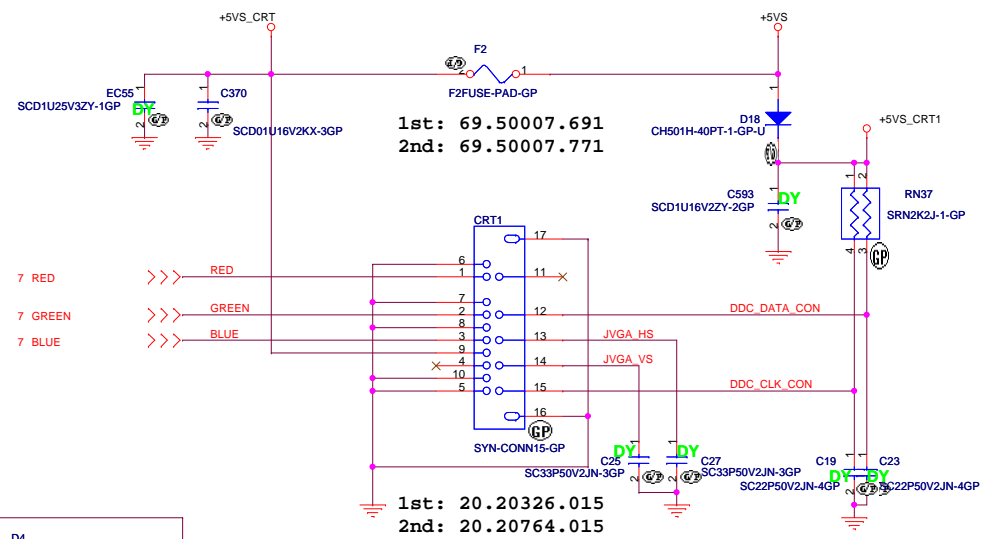
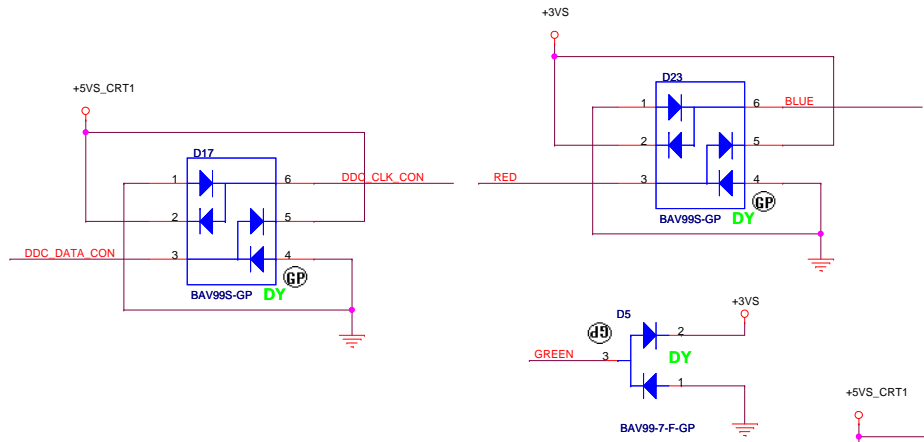
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2-SODIMM SLOT1**

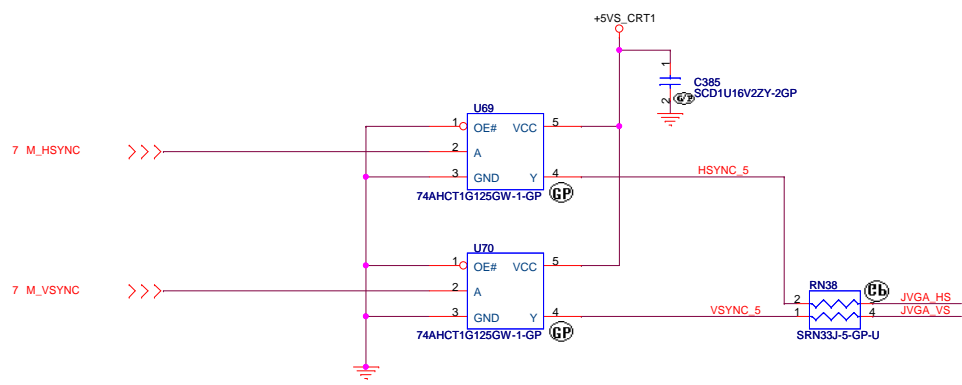
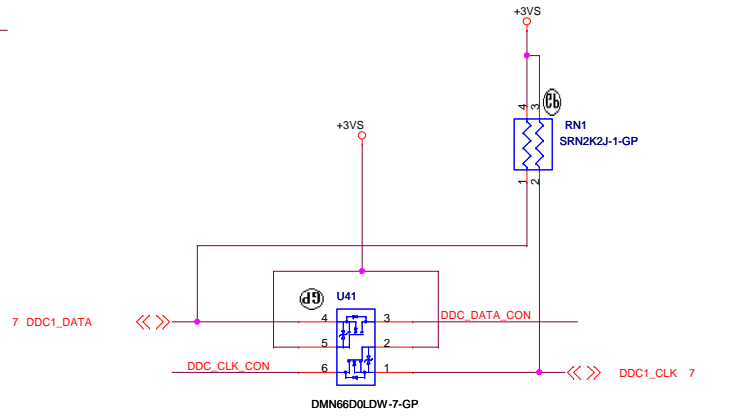
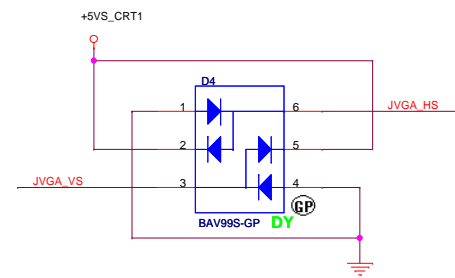
Doc Number: **HBU16 1.2**

Date: Thursday, July 09, 2009 Sheet 12 of 41

CRT I/F & CONNECTOR



Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



5V @ ext. CRT side

<Core Design>

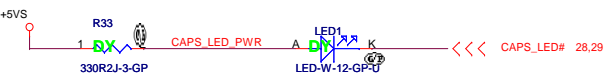
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

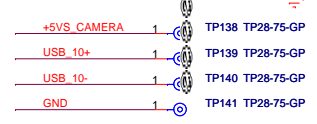
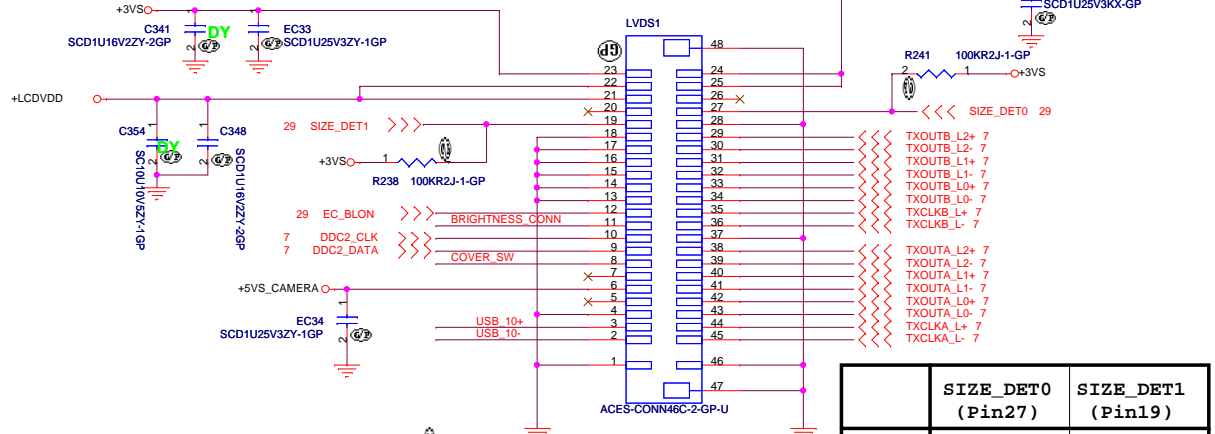
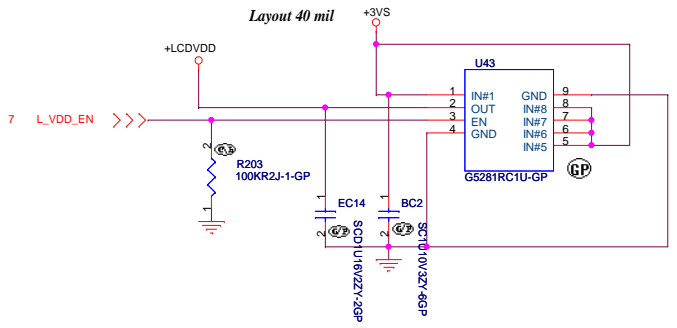
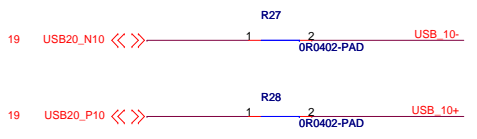
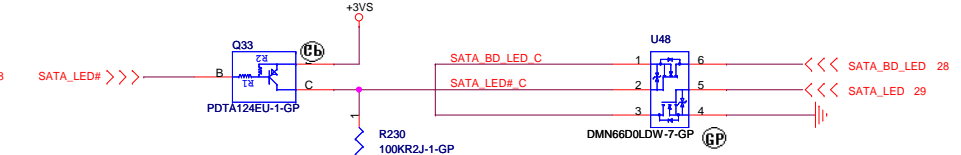
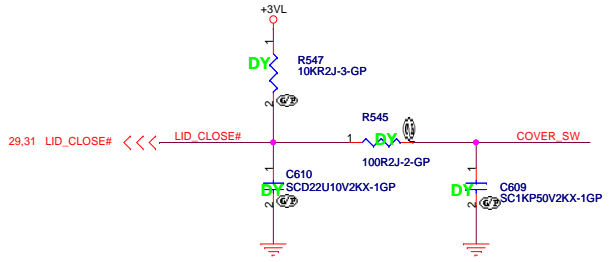
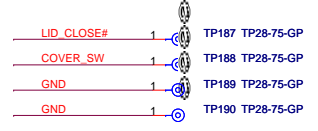
Size A3 Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 14 of 41

LCD / INVERTER INTERFACE / CAMERA

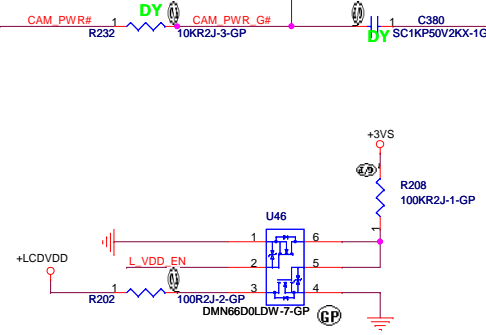
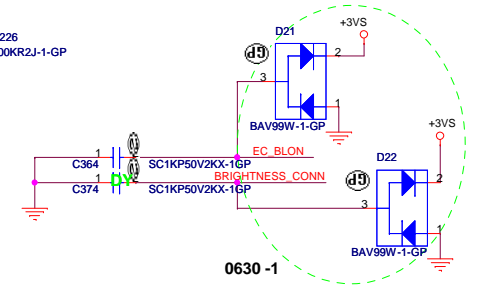
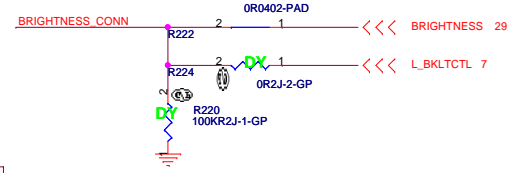
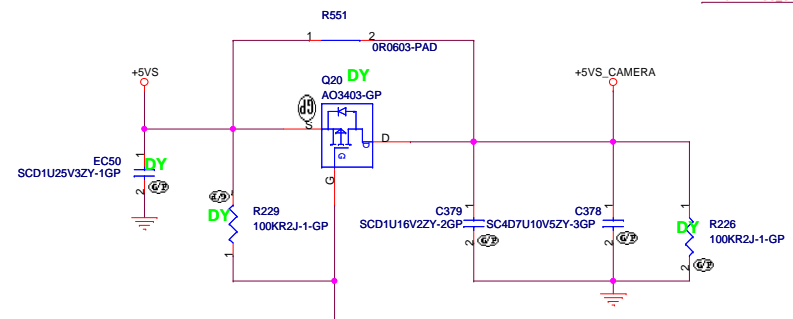


White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70



1st: 20.F1296.046
 2nd: 20.F1270.046

	SIZE_DET0 (Pin27)	SIZE_DET1 (Pin19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0



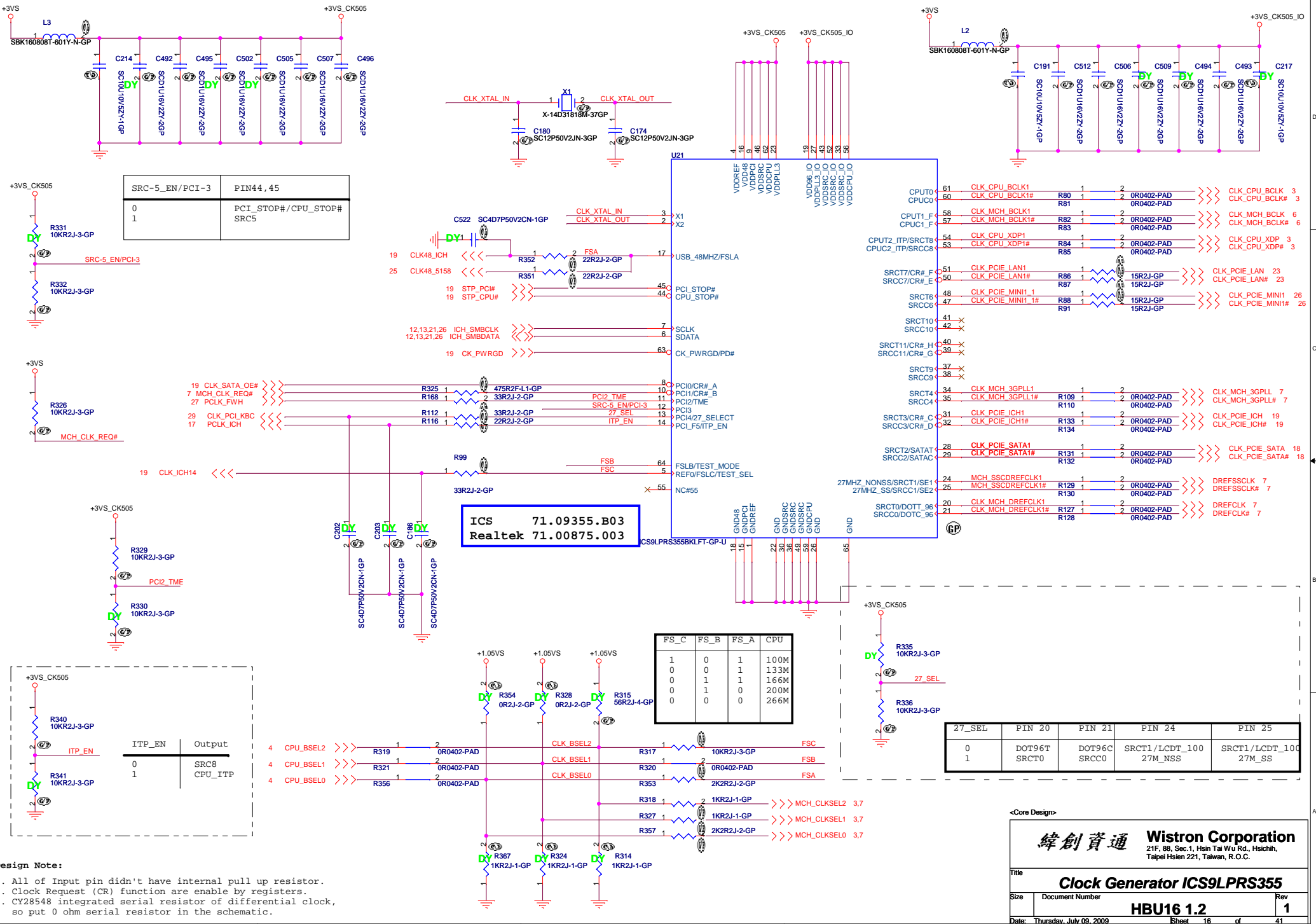
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector/CAM/LED**

Size A3 Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 15 of 41



SRC-5_EN/PCI-3	PIN44, 45
0	PCI_STOP#/CPU_STOP#
1	SRC5

ICS 71.09355.B03
Realtek 71.00875.003

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M
0	0	0	266M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDDT_100	SRCT1/LCDDT_100
1			27M_NSS	27M_SS

Design Note:

- All of Input pin didn't have internal pull up resistor.
- Clock Request (CR) function are enable by registers.
- CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

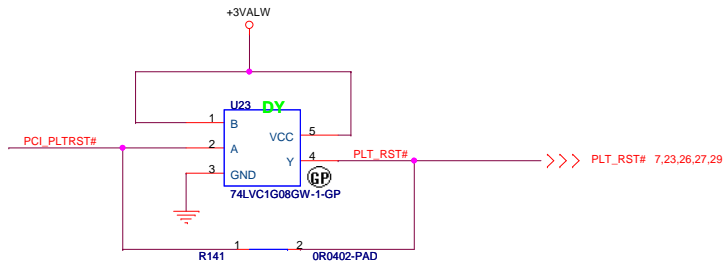
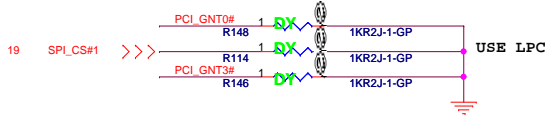
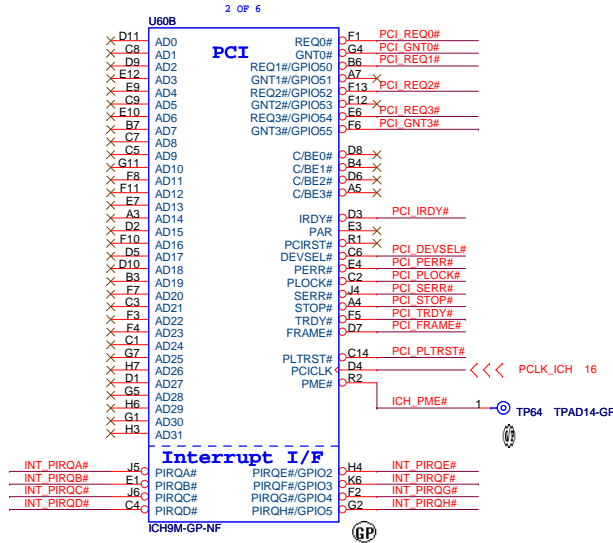
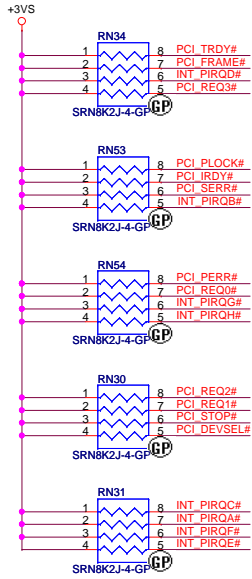
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien T21, Taiwan, R.O.C.

Title: **Clock Generator ICS9LPRS355**

Size: Document Number **HBU16 1.2** Rev **1**

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BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

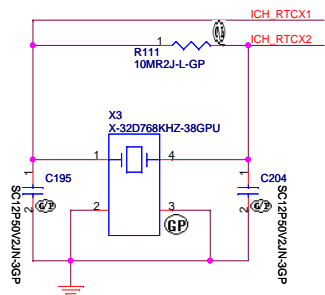
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (1 of 5)**

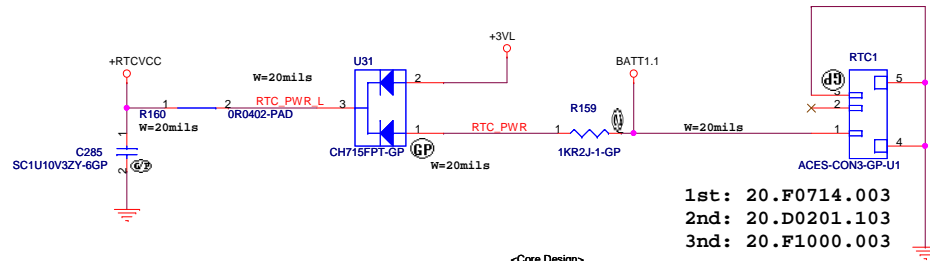
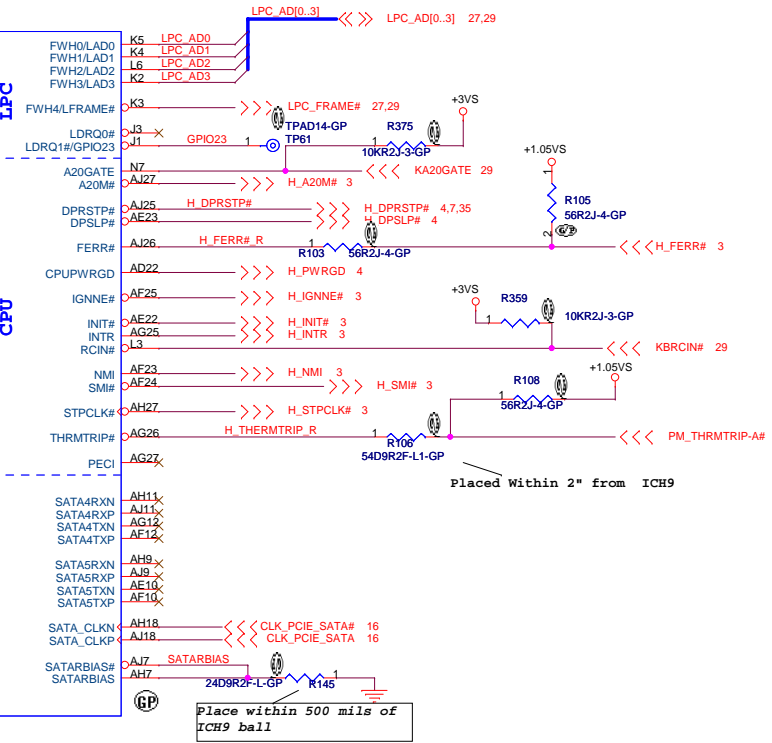
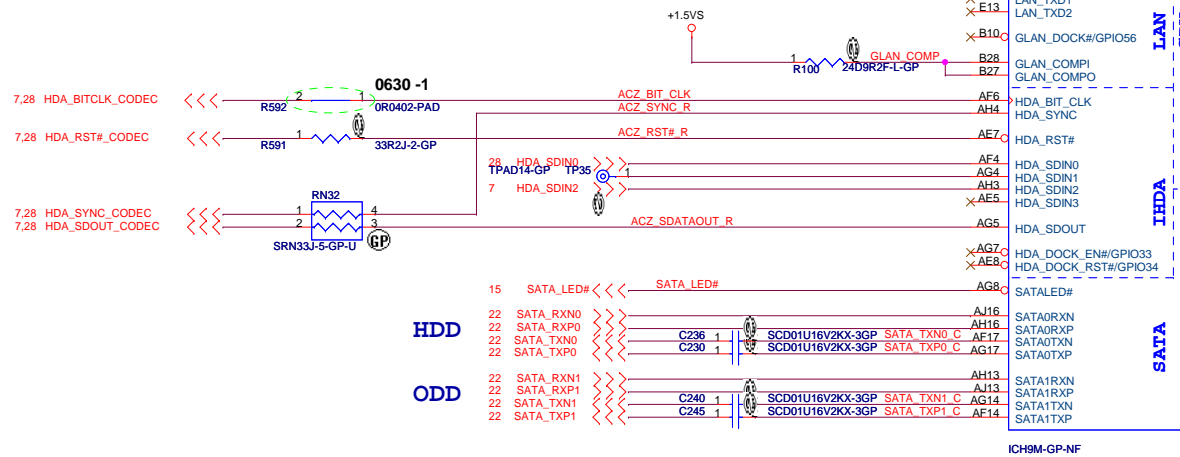
Size: Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 17 of 41



32.768Khz 12.5pf 10ppm
 1st: 82.30001.691 (KDS)
 2nd: 82.30001.861 (EPSON)

GLAN_COMP place within 500 mil of ICH9M



1st: 20.F0714.003
 2nd: 20.D0201.103
 3rd: 20.F1000.003

integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

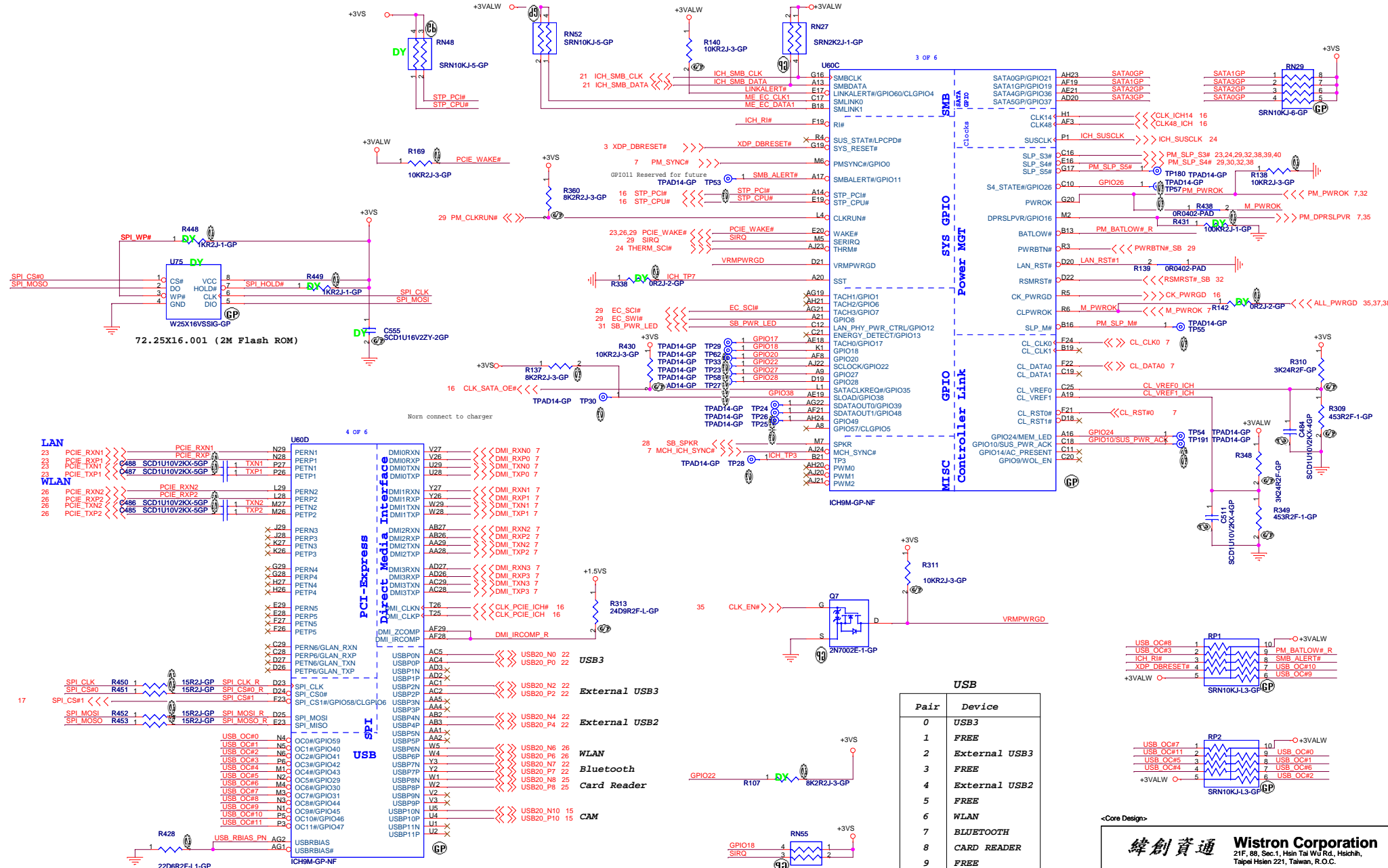
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (2 of 5)**

Size: Document Number **HBU16.1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 18 of 41



Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD READER
9	FREE
10	CAMERA
11	FREE

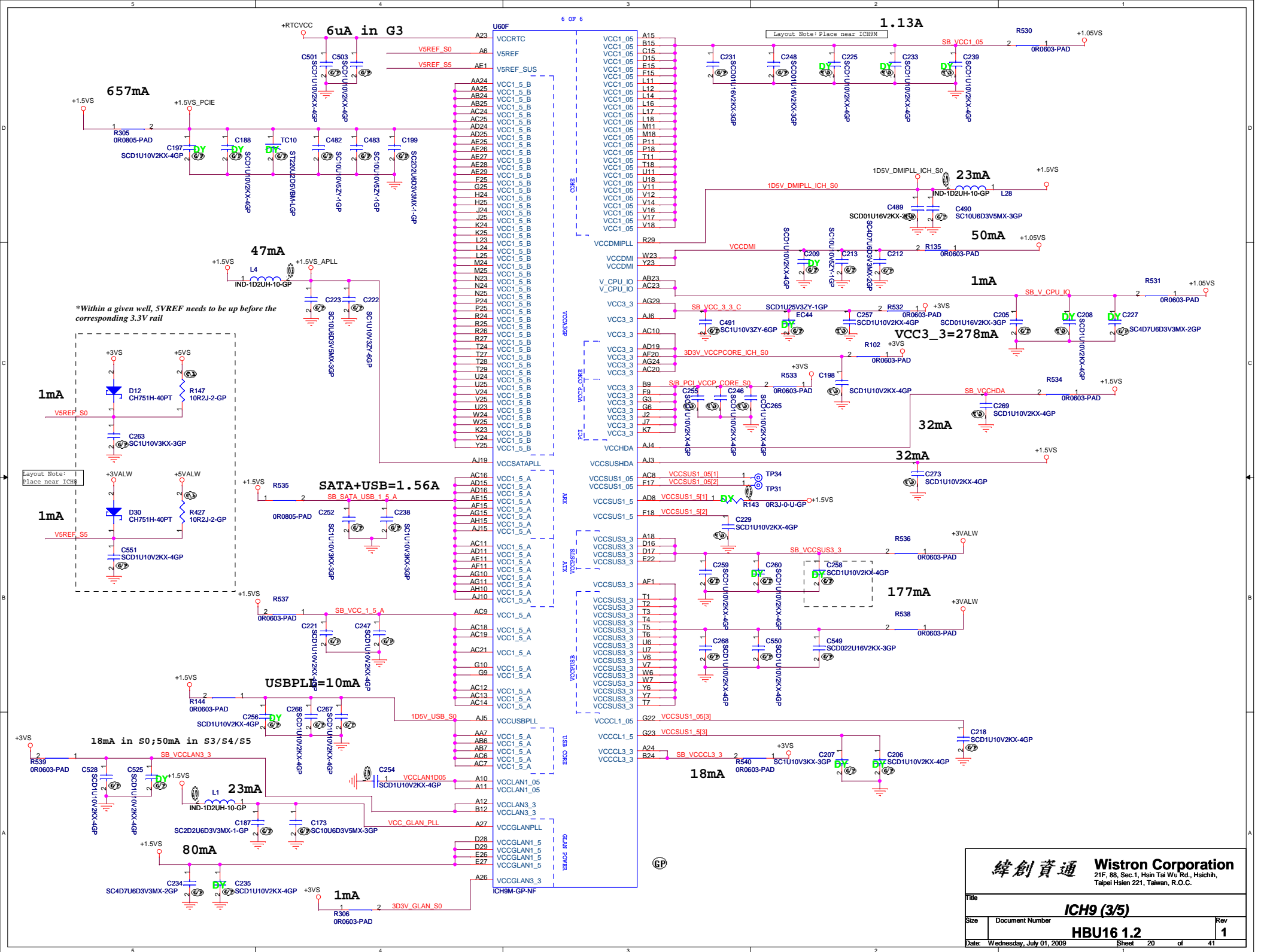
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **ICH9-M (2 of 5)**

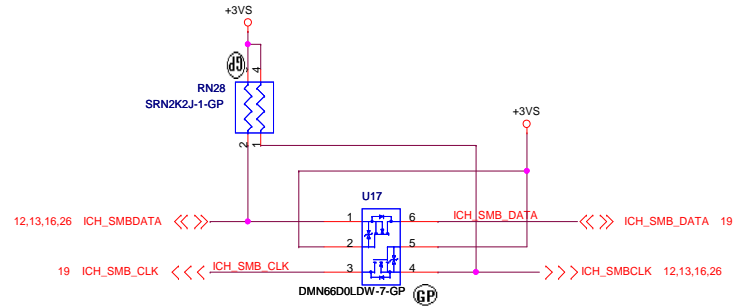
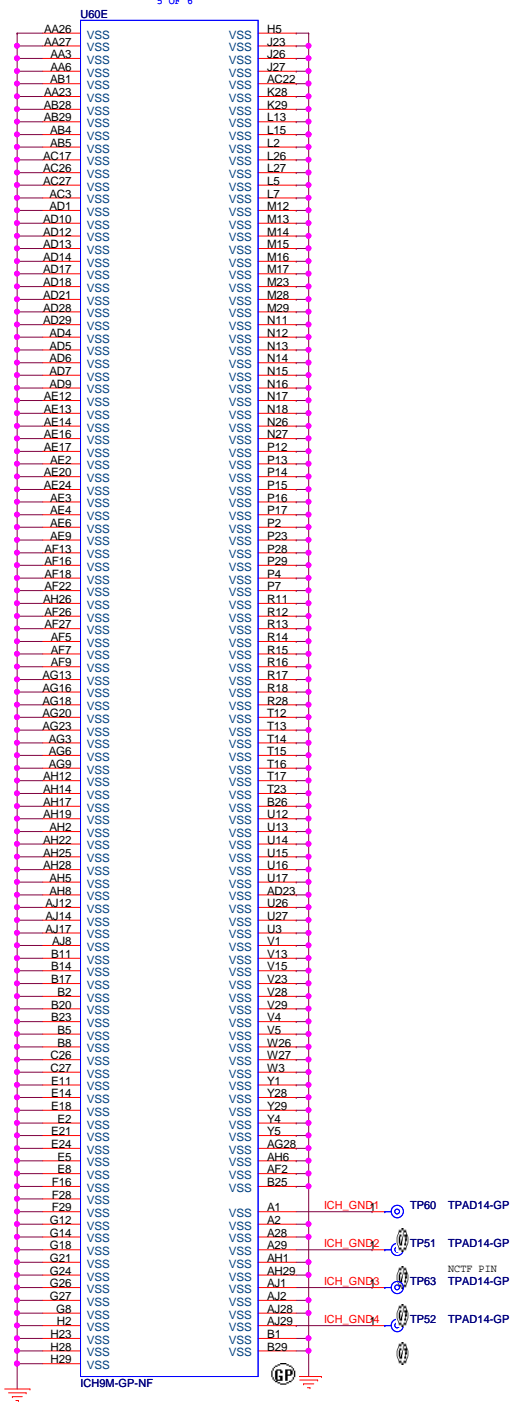
Size: Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 19 of 41



緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

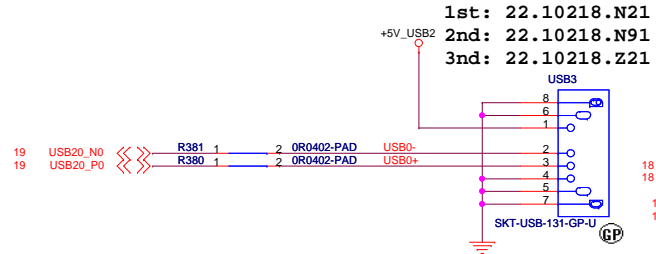
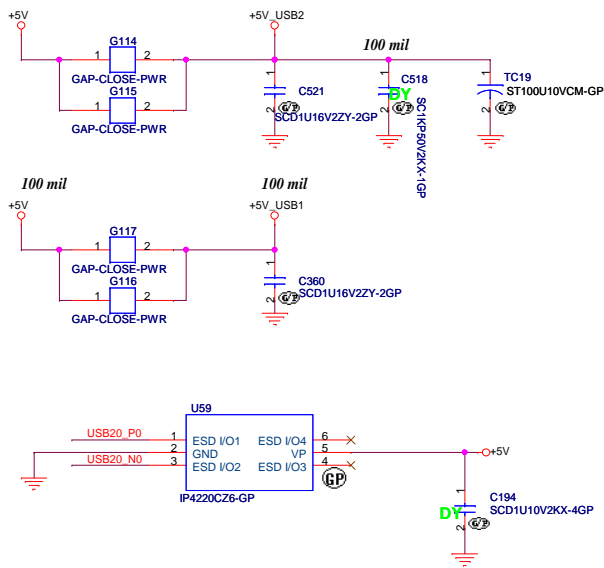
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Size	Document Number	HBU16 1.2	
		Rev 1	
Date: Wednesday, July 01, 2009	Sheet 20	of 41	



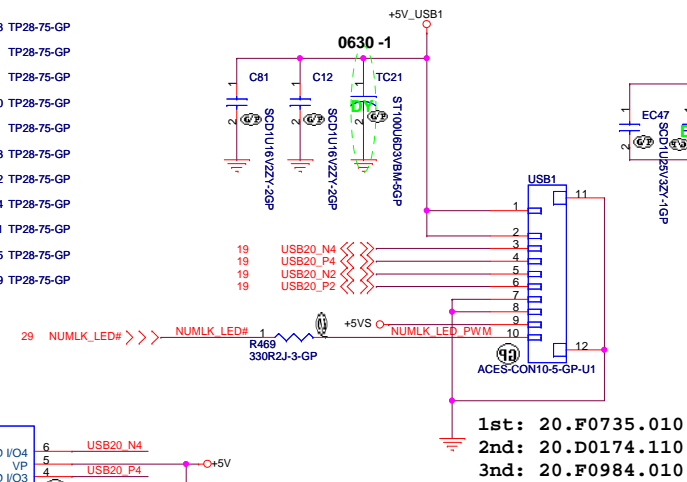
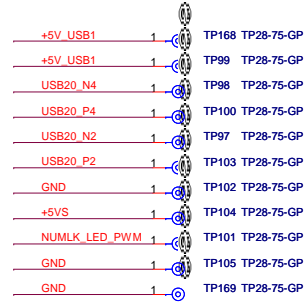
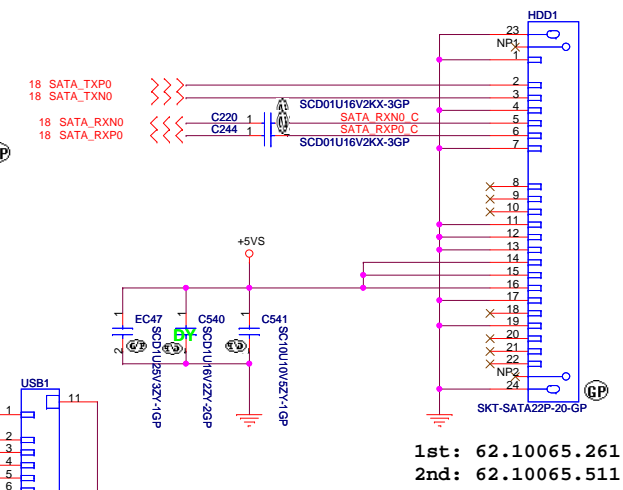
SMBUS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
ICH9-M (4 of 4)		
Size	Document Number	Rev
	HBU16 1.2	1
Date:	Thursday, July 09, 2009	Sheet 21 of 41

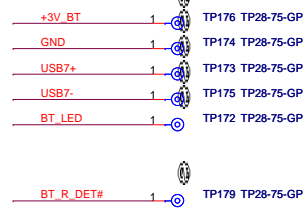
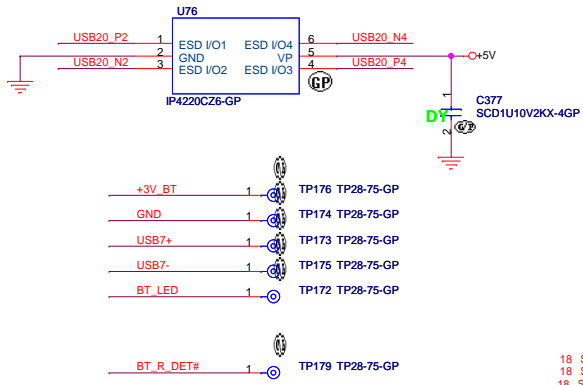
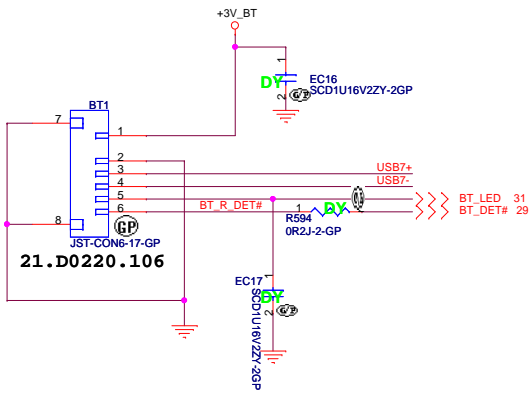
USB PORT



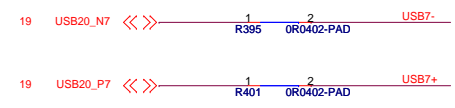
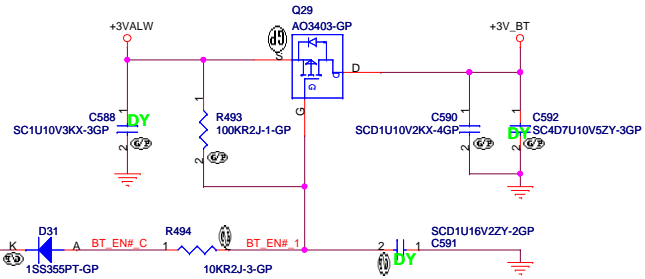
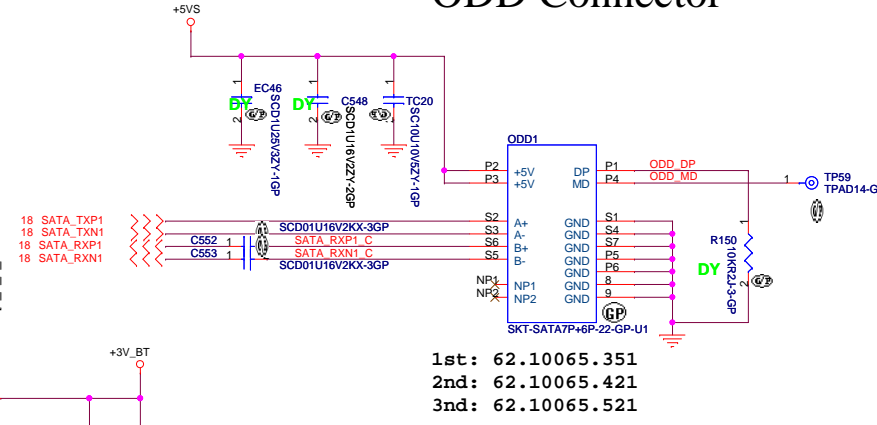
SATA HDD Connector



BLUETOOTH



ODD Connector

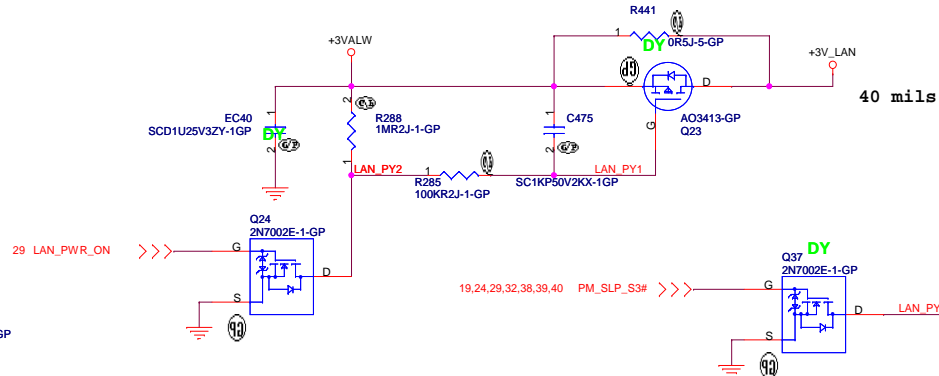
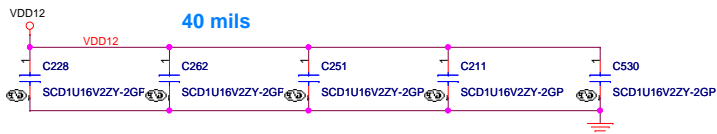
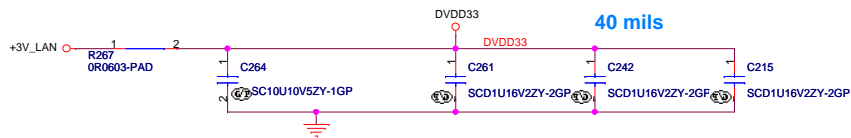


- 1st: 62.10065.351
- 2nd: 62.10065.421
- 3rd: 62.10065.521

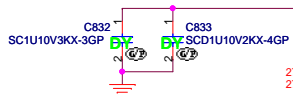
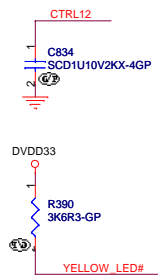
<Core Design>

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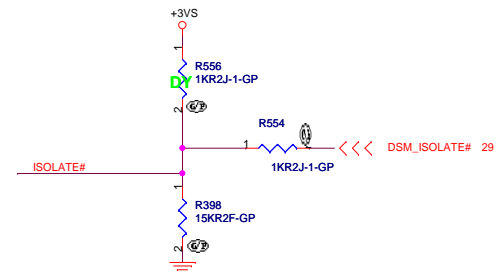
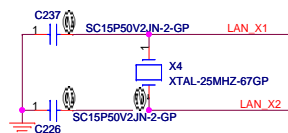
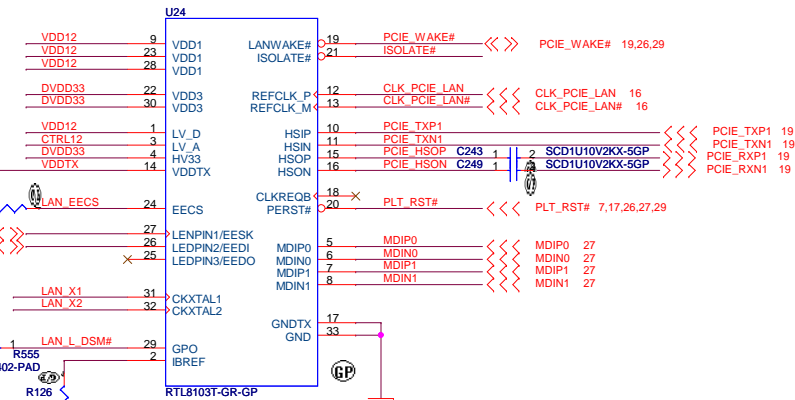
Title		
HDD/CDROM/USB/BT		
Size	Document Number	Rev
A3	HBU16 1.2	1
Date:	Thursday, July 09, 2009	Sheet 22 of 41



EEPROM LED OPTION USE '01'
 (DEFINED IN SPEC)
 => LED1 : LINK (Green)
 => LED2 : ACT (Yellow)
 (BOTH 10/100 AND GIGA CHIP)



27 GREEN_LED#
 27 YELLOW_LED#



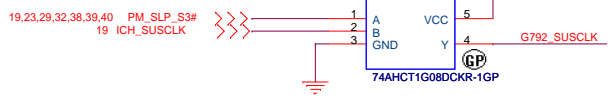
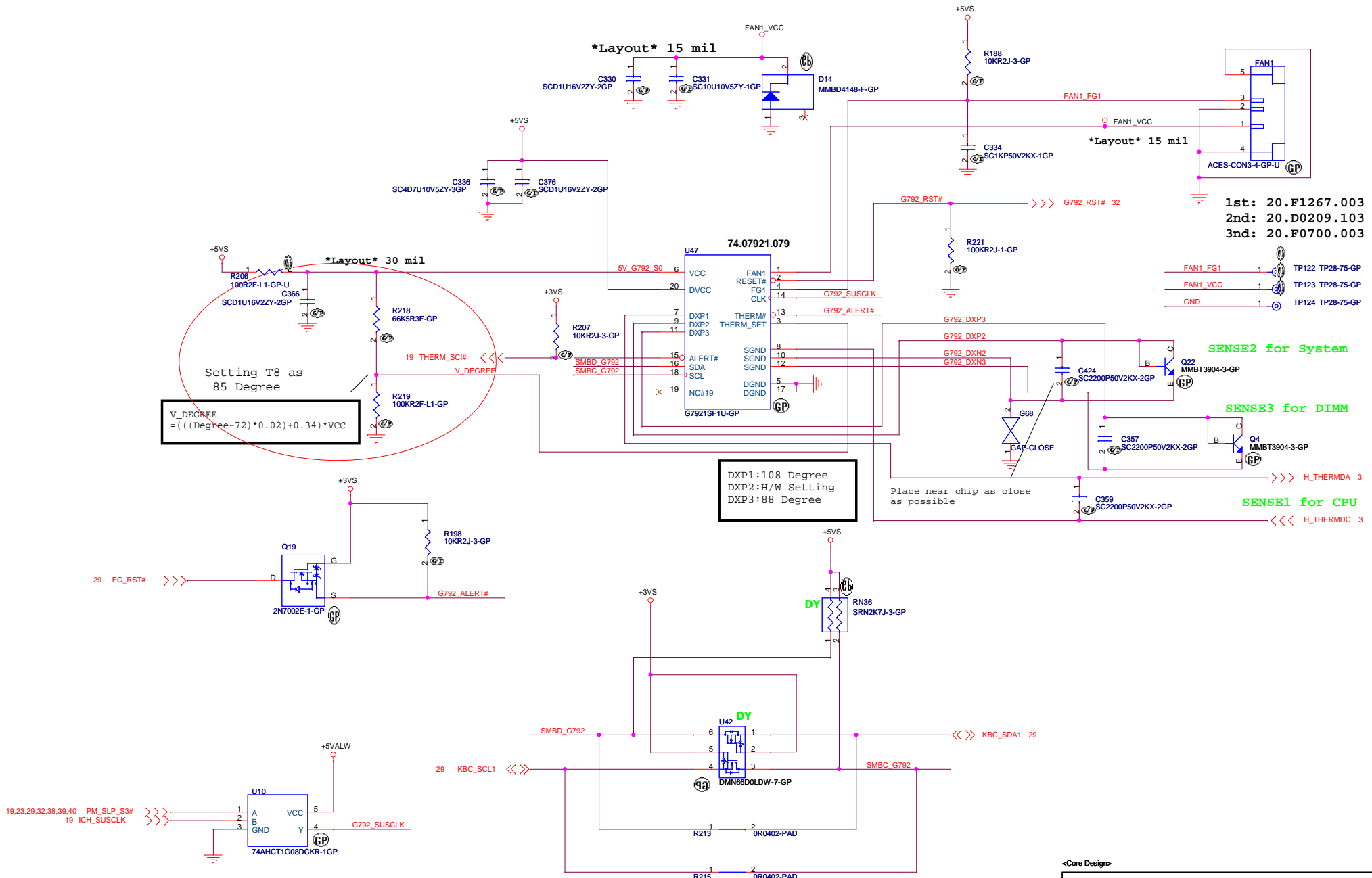
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緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8103T**

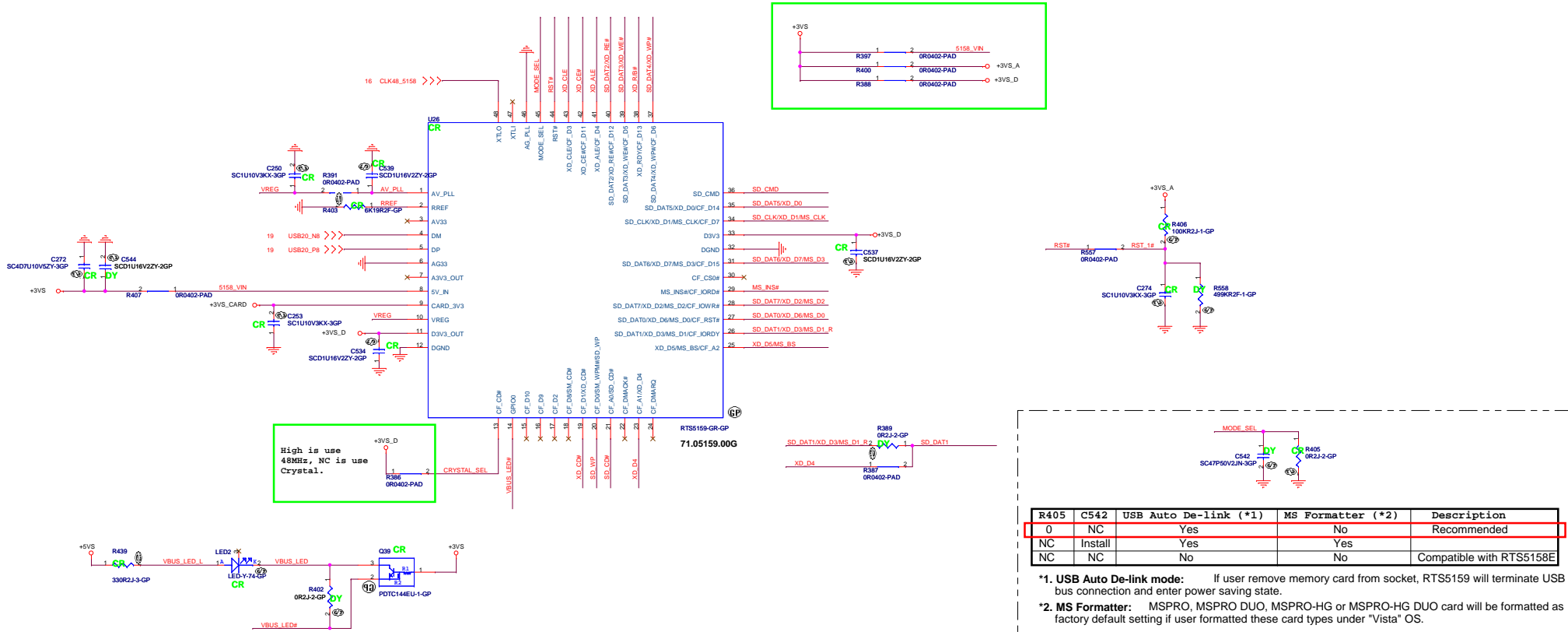
Size A3 Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 23 of 41

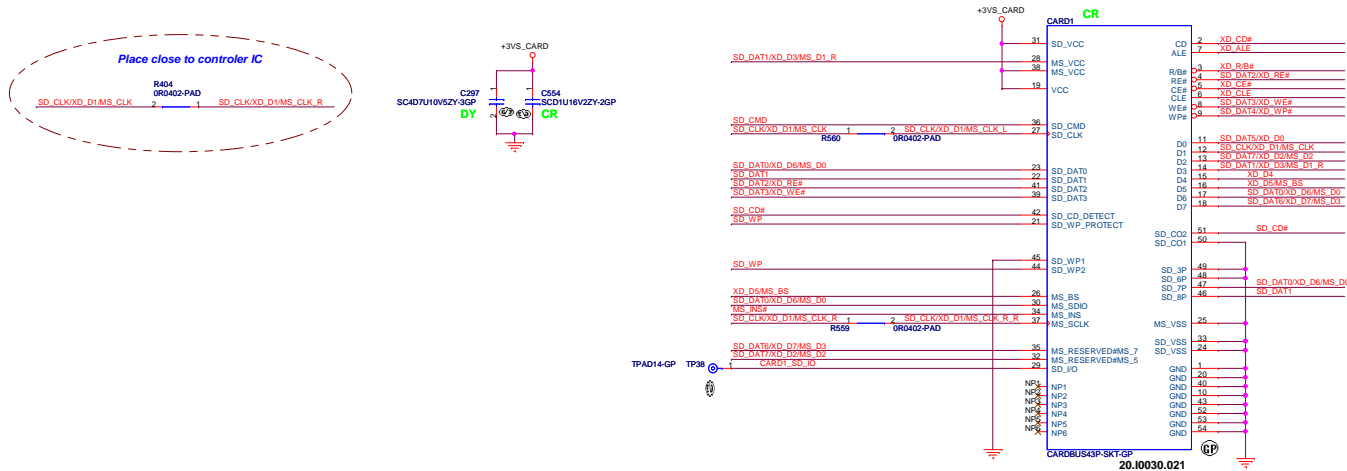


<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsten 221, Taiwan, R.O.C.		
Title		
Thermal/Fan Controller		
Size	Document Number	Rev
Custom	HBU16 1.2	1
Date: Thursday, July 09, 2009	Sheet 24 of	41

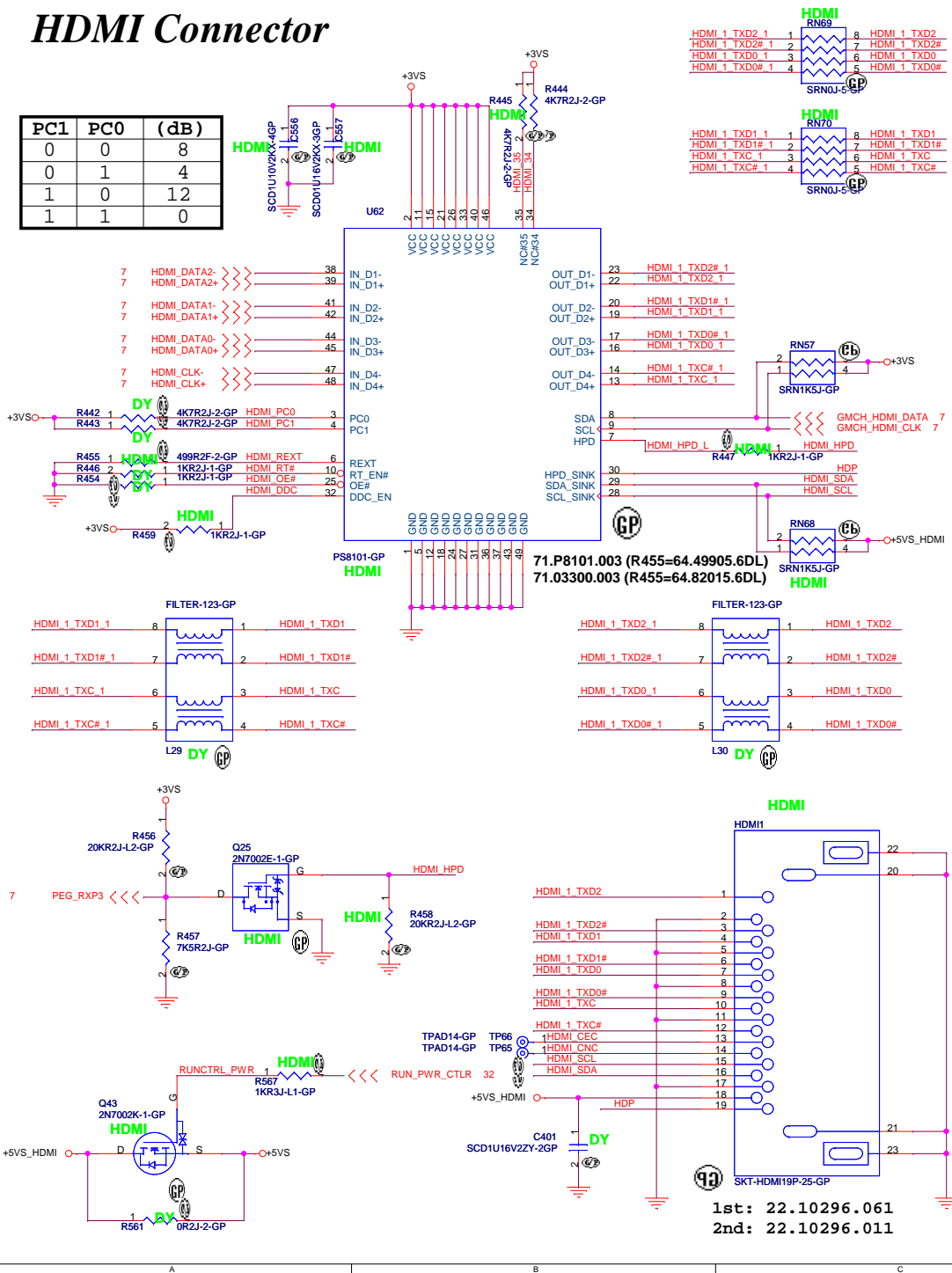


4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



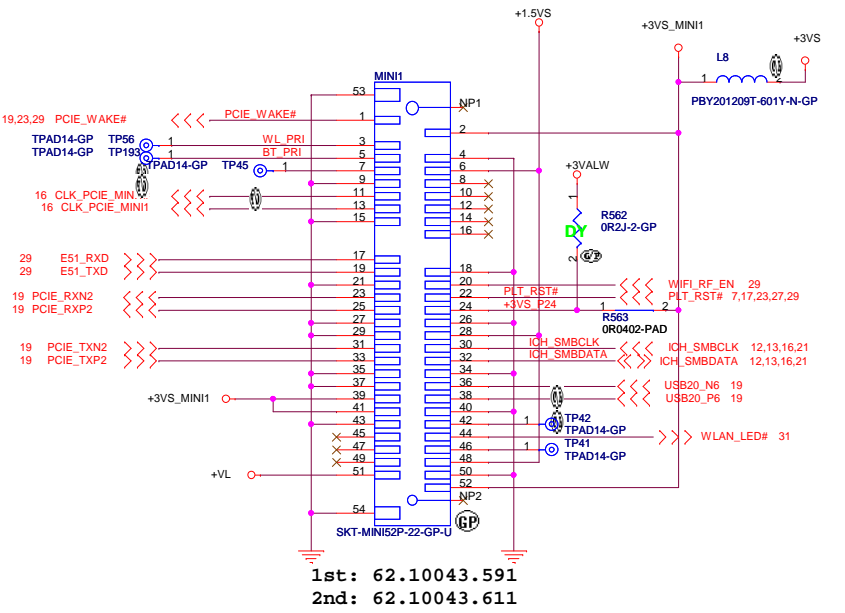
HDMI Connector

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0

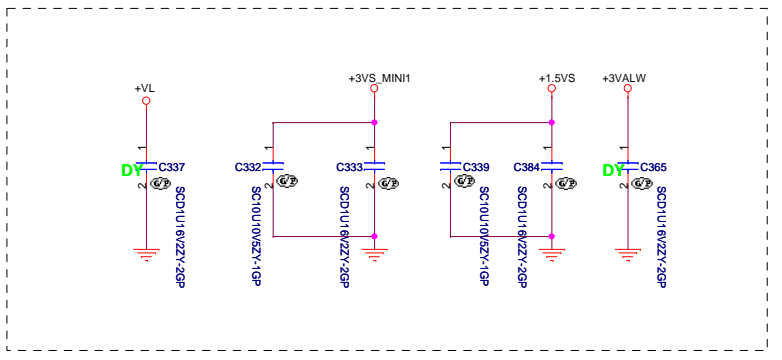


1st: 22.10296.061
2nd: 22.10296.011

Mini Card Connector1(802.11a/b/g)



1st: 62.10043.591
2nd: 62.10043.611



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD/HDMI CONN.**

Size A3 Document Number: **HBU16 1.2** Rev: **1**

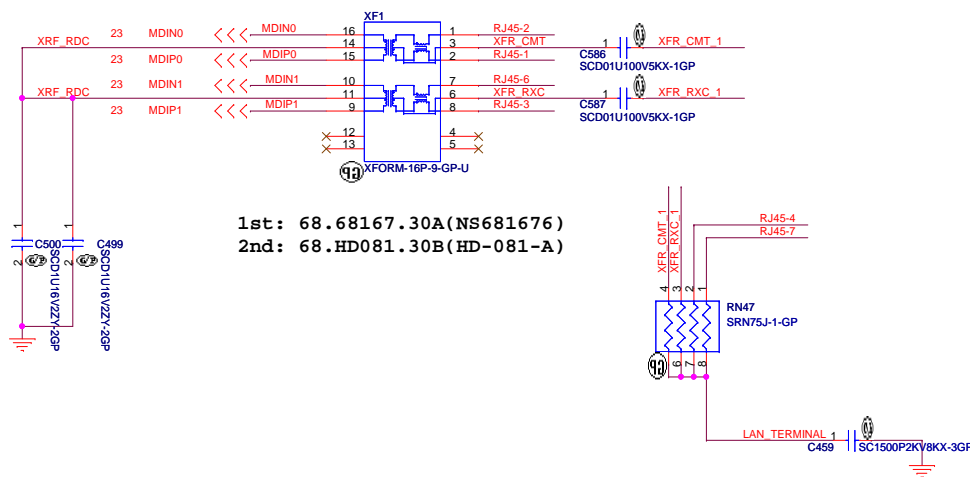
Date: Thursday, July 09, 2009 Sheet 26 of 41

LAN Connector

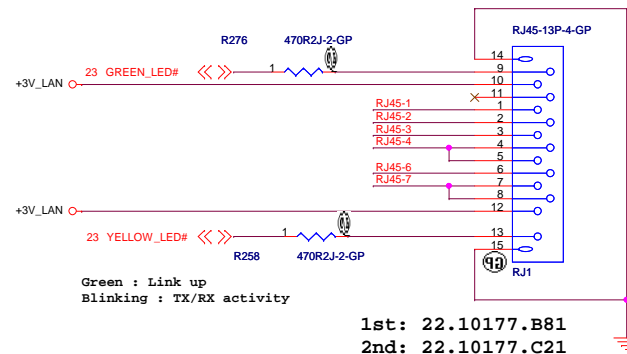
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW

10/100M Lan Transformer



1st: 68.68167.30A(NS681676)
2nd: 68.HD081.30B(HD-081-A)



Green : Link up
Blinking : TX/RX activity

1st: 22.10177.B81
2nd: 22.10177.C21

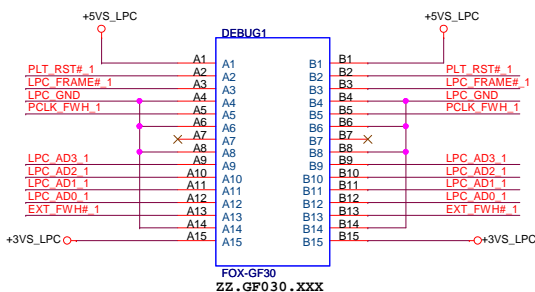
Remark:
Add trace width to 20mils for RJ1 pin4, 5 and pin 7, 8.

Golden Finger for Debug Board

TOP VIEW (A)

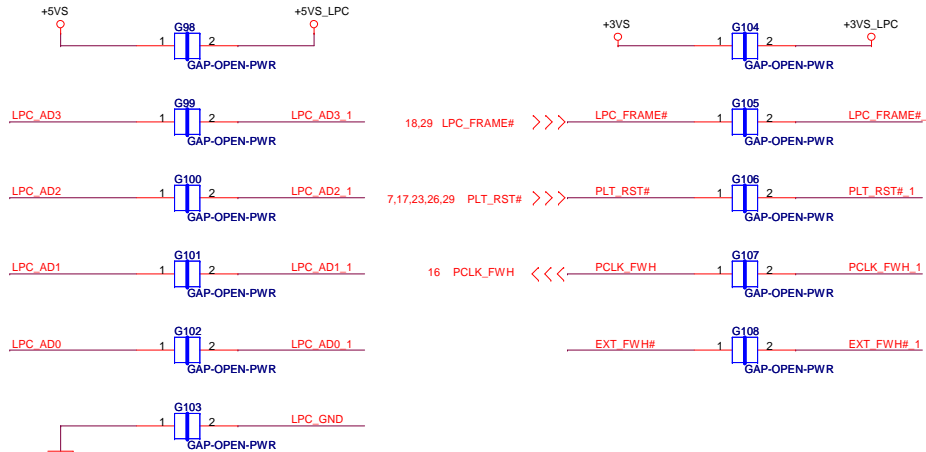
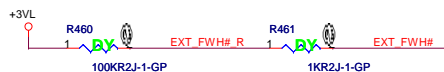
A15 (B1)
A14 (B2)
:
:
:
A2 (B14)
A1 (B15)

BOTTOM VIEW (B)



Please put near board edge.

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



<Core Design>

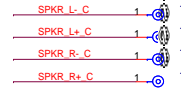
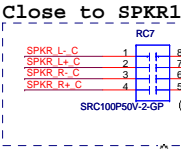
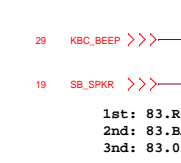
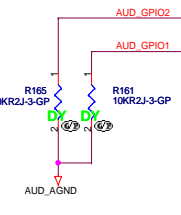
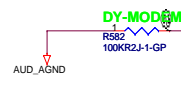
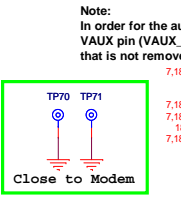
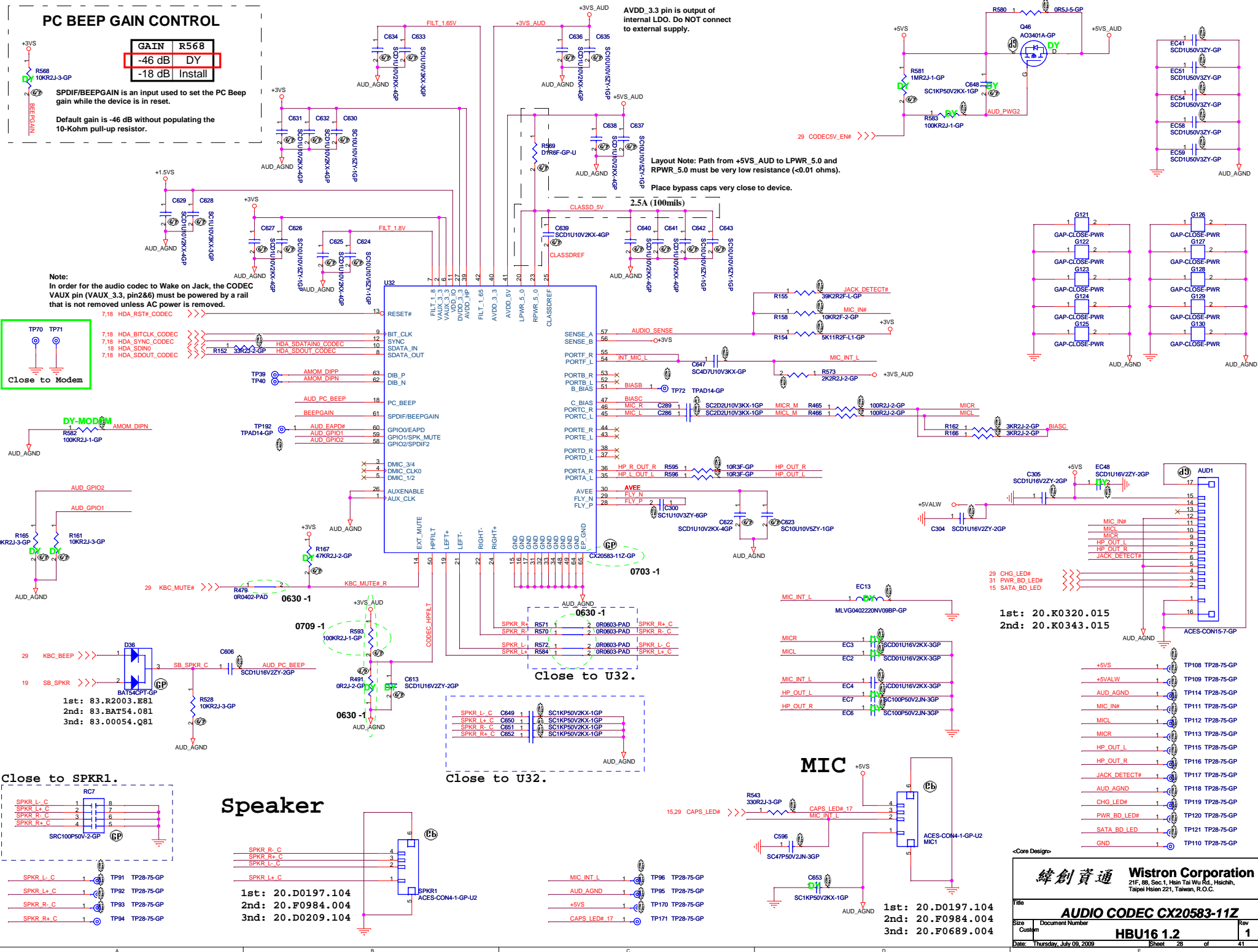
緯創資通 Wistron Corporation	
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Title	LAN CONN/Debug
Size A3	Document Number
Date: Thursday, July 09, 2009	HBU16 1.2
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of 41	

PC BEEP GAIN CONTROL

GAIN	R568
-46 dB	DY
-18 dB	Install

SPDIF/BEEPGAIN is an input used to set the PC BEEP gain while the device is in reset.

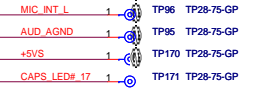
Default gain is -46 dB without populating the 10-Kohm pull-up resistor.



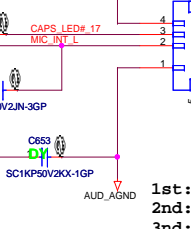
Speaker

- 1st: 20.D0197.104
- 2nd: 20.F0984.004
- 3nd: 20.D0209.104

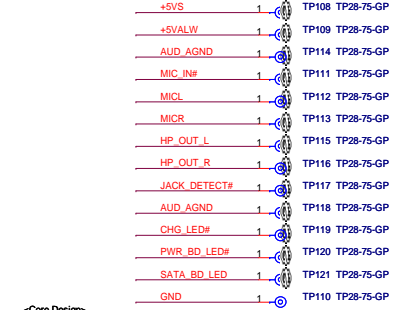
Close to U32.



MIC



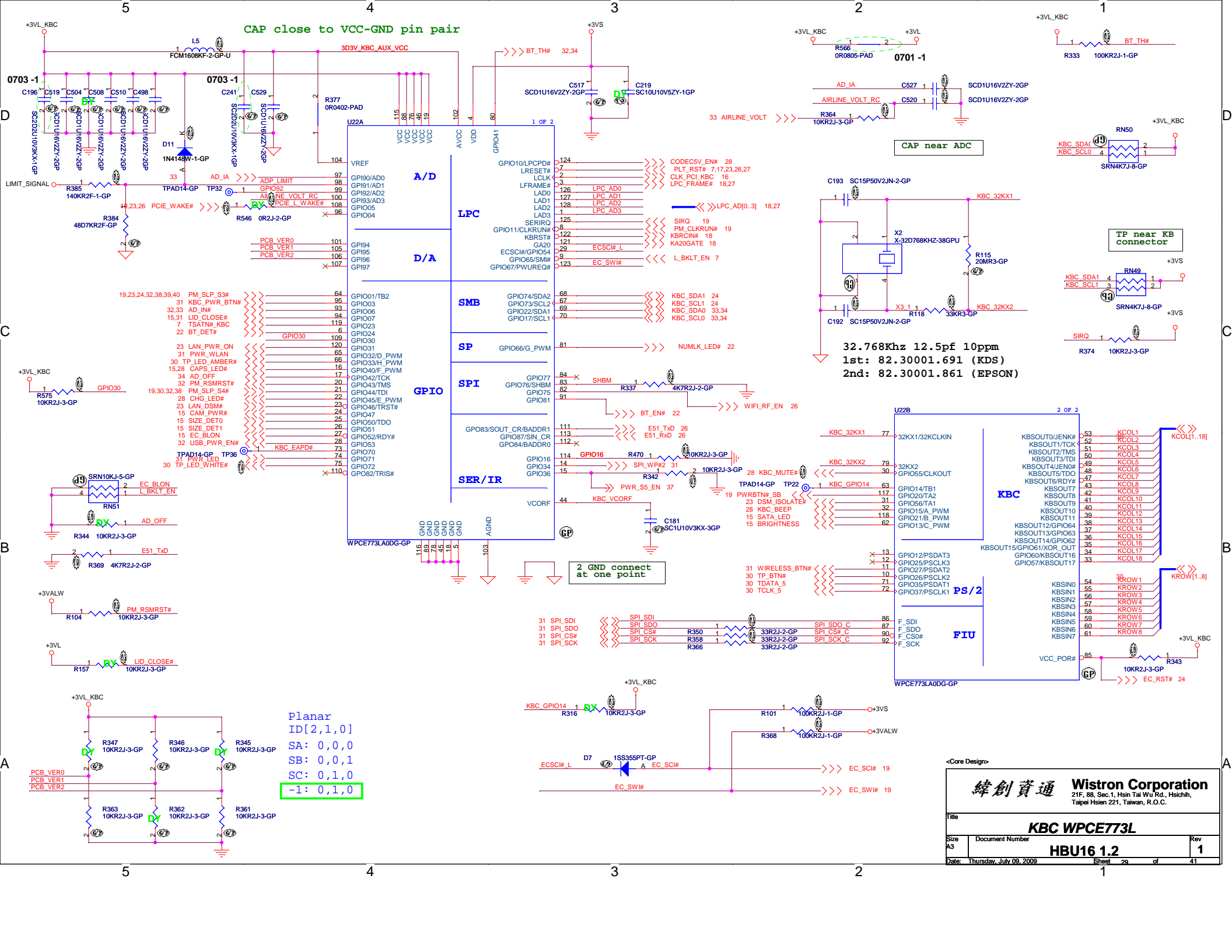
- 1st: 20.K0320.015
- 2nd: 20.K0343.015



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AUDIO CODEC CX20583-11Z

File: HBU16 1.2
Size: Custom Document Number: 1
Date: Thursday, July 09, 2009 Sheet: 28 of 41



CAP close to VCC-GND pin pair

CAP near ADC

TP near KB connector

2 GND connect at one point

Planar
ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,0

31	SPI_SDI	86	F_SDI
31	SPI_SDO	87	F_SDO
31	SPI_CS#	90	F_CS#
31	SPI_SCK	92	F_SCK

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KBC WPCE773L

Size A3 Document Number HBU16 1.2 Rev 1

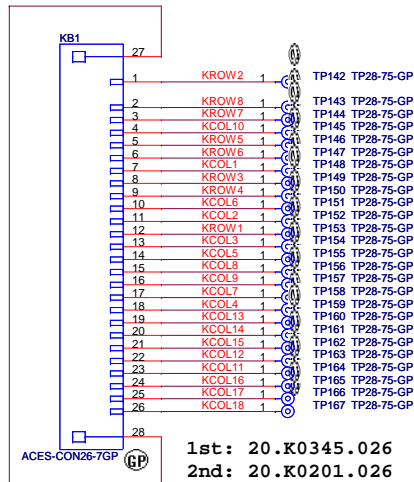
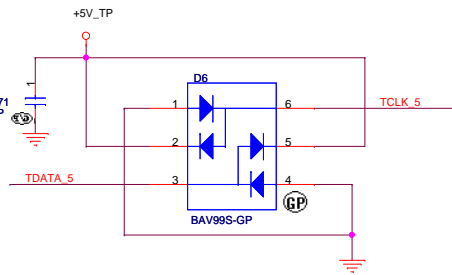
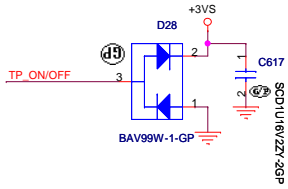
Date: Thursday, July 09, 2009 Sheet 29 of 41

Internal Keyboard Connector

29 KROW[1..8] <<<<
29 KCOL[1..18] <<<<

Keyboard matrix (from vendor)

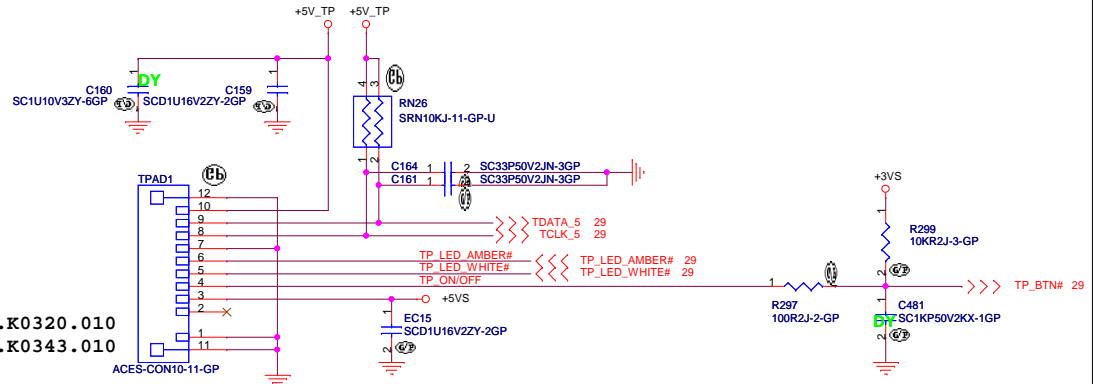
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



1st: 20.K0345.026
2nd: 20.K0201.026

GND 1 TP185 TP28-75-GP
GND 1 TP186 TP28-75-GP

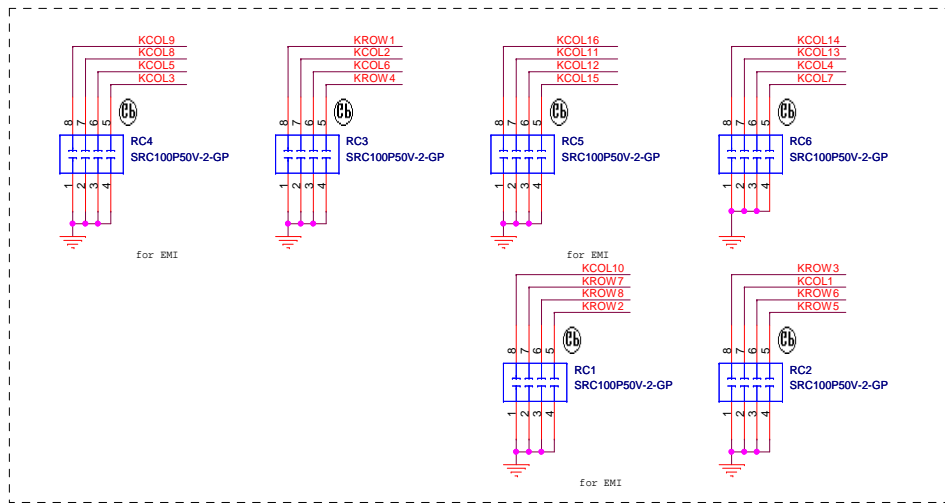
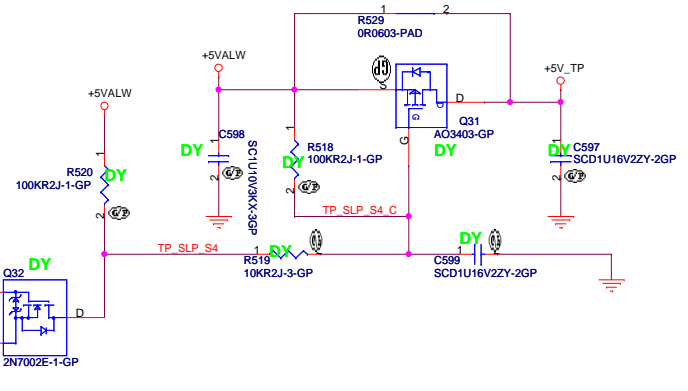
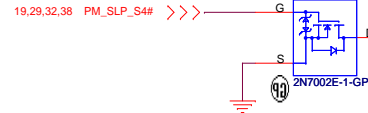
TouchPad Connector

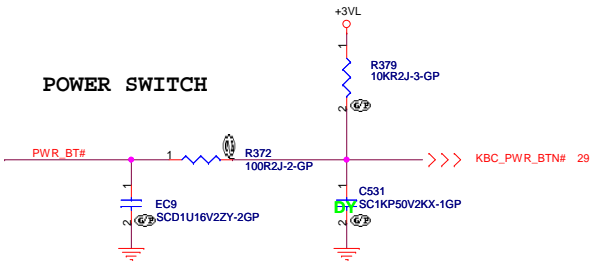
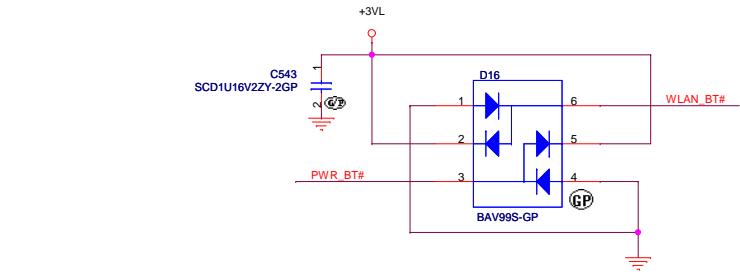
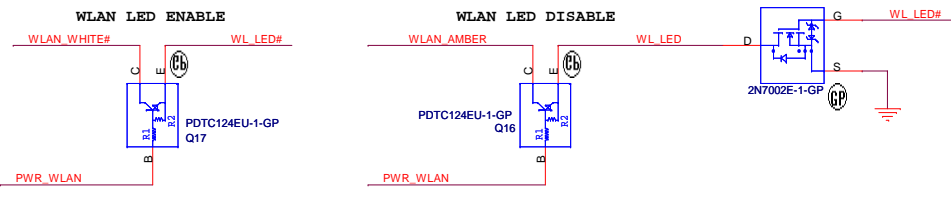
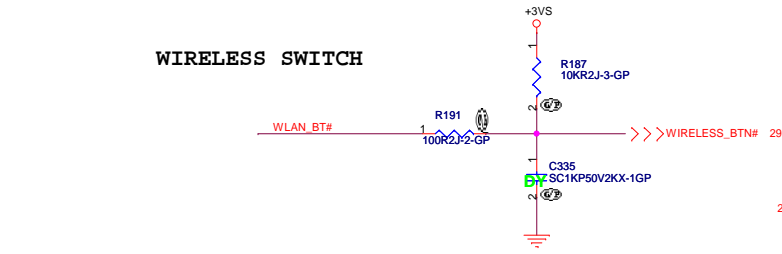
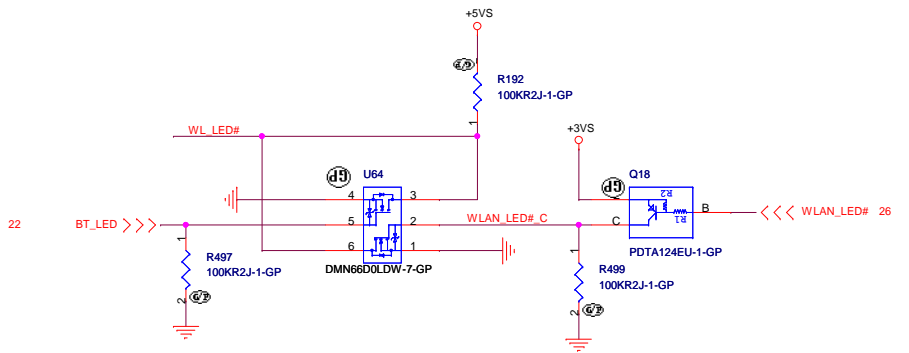
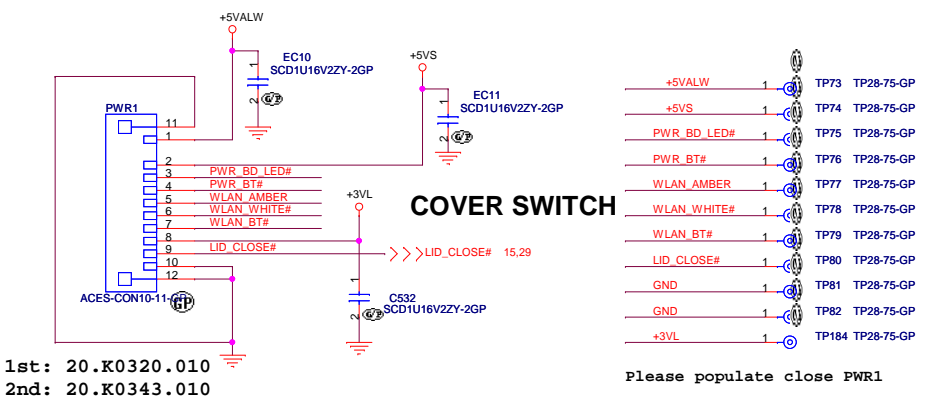
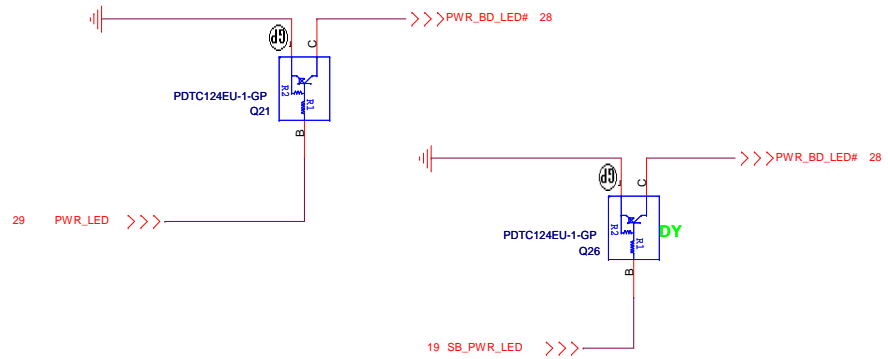
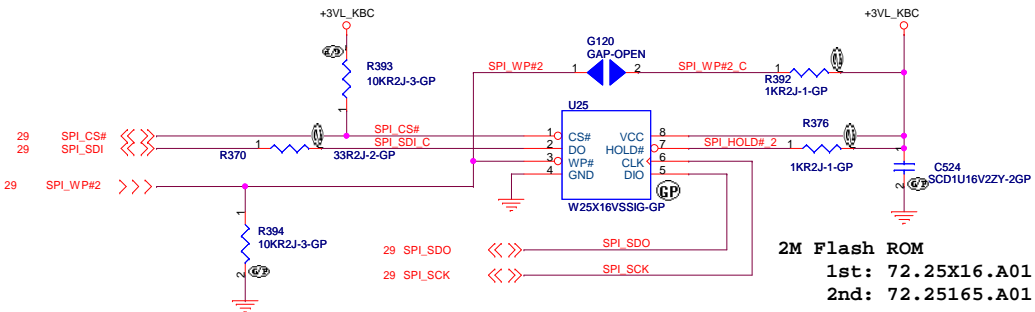


1st: 20.K0320.010
2nd: 20.K0343.010

+5V_TP 1 TP83 TP28-75-GP
TDATA_5 1 TP84 TP28-75-GP
TCLK_5 1 TP85 TP28-75-GP
GND 1 TP106 TP28-75-GP
TP_LED_AMBER# 1 TP86 TP28-75-GP
TP_LED_WHITE# 1 TP87 TP28-75-GP
GND 1 TP107 TP28-75-GP
TP_ON/OFF 1 TP88 TP28-75-GP
+5VS 1 TP89 TP28-75-GP
GND 1 TP90 TP28-75-GP

Please populate close TPAD1





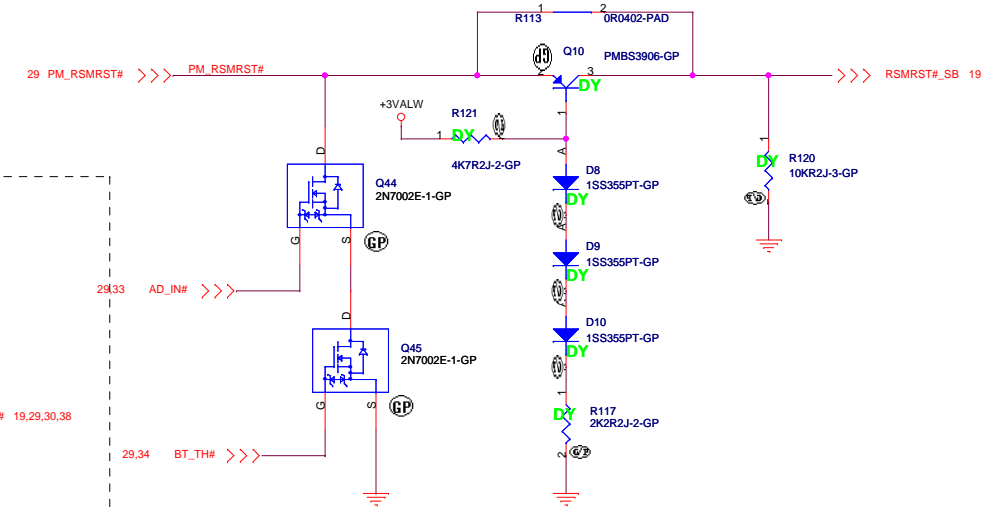
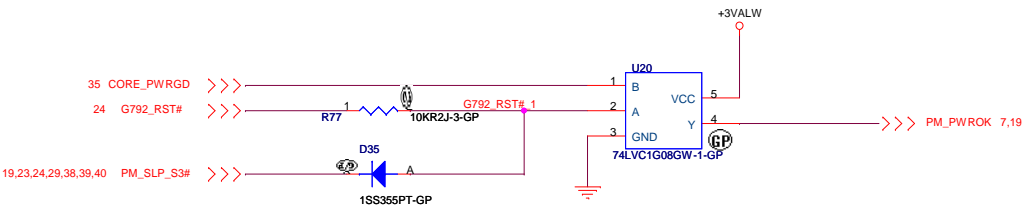
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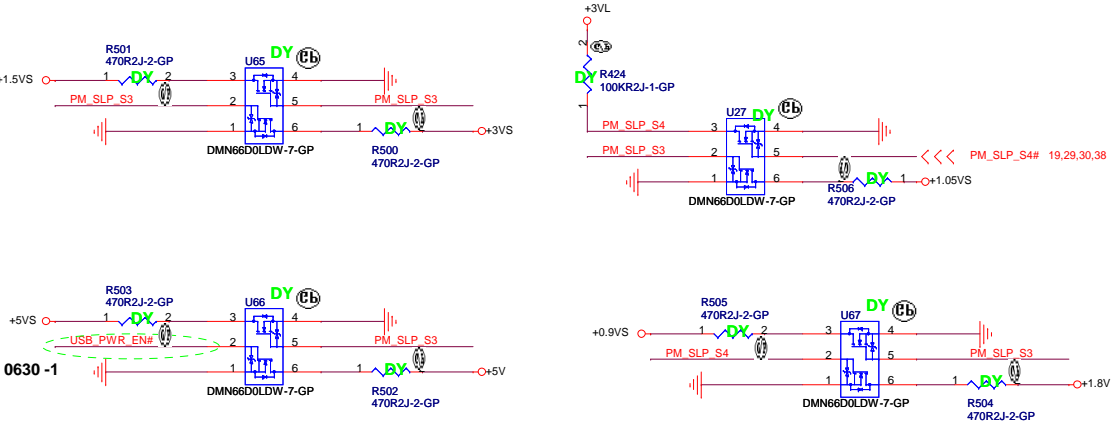
Title: **FWH and CONN.**

Size A3 Document Number **HBU16 1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 31 of 41



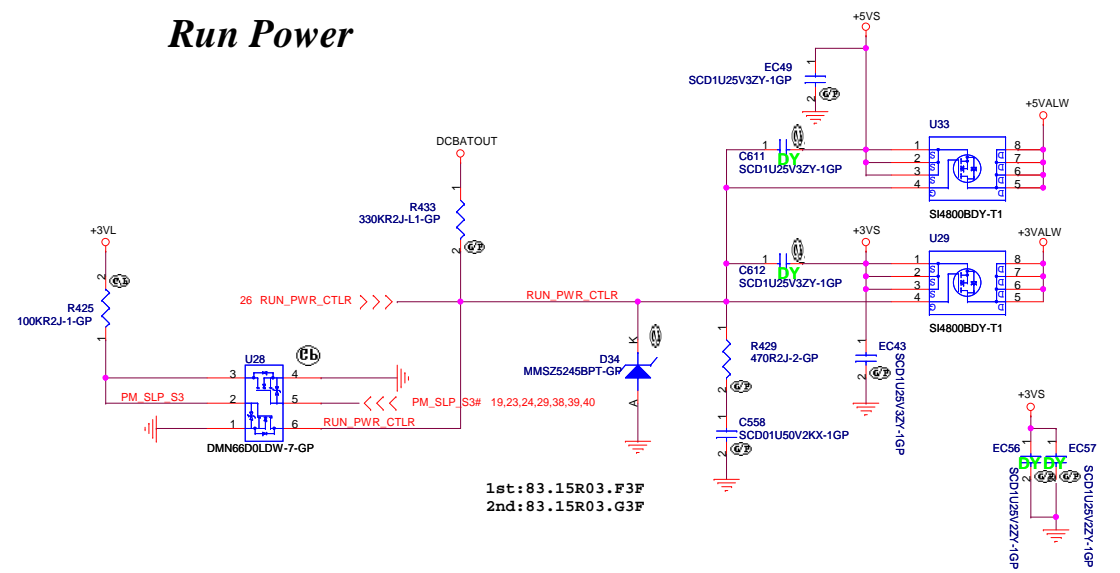
Discharge Circuit



0523 SF

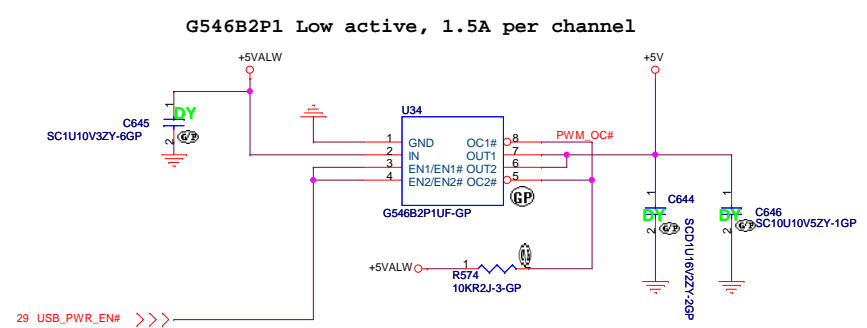
+5VALW to +5VS Transfer +3VALW to +3VS Transfer

Run Power



1st: 83.15R03.F3F
2nd: 83.15R03.G3F

+5VALW to +5V Transfer



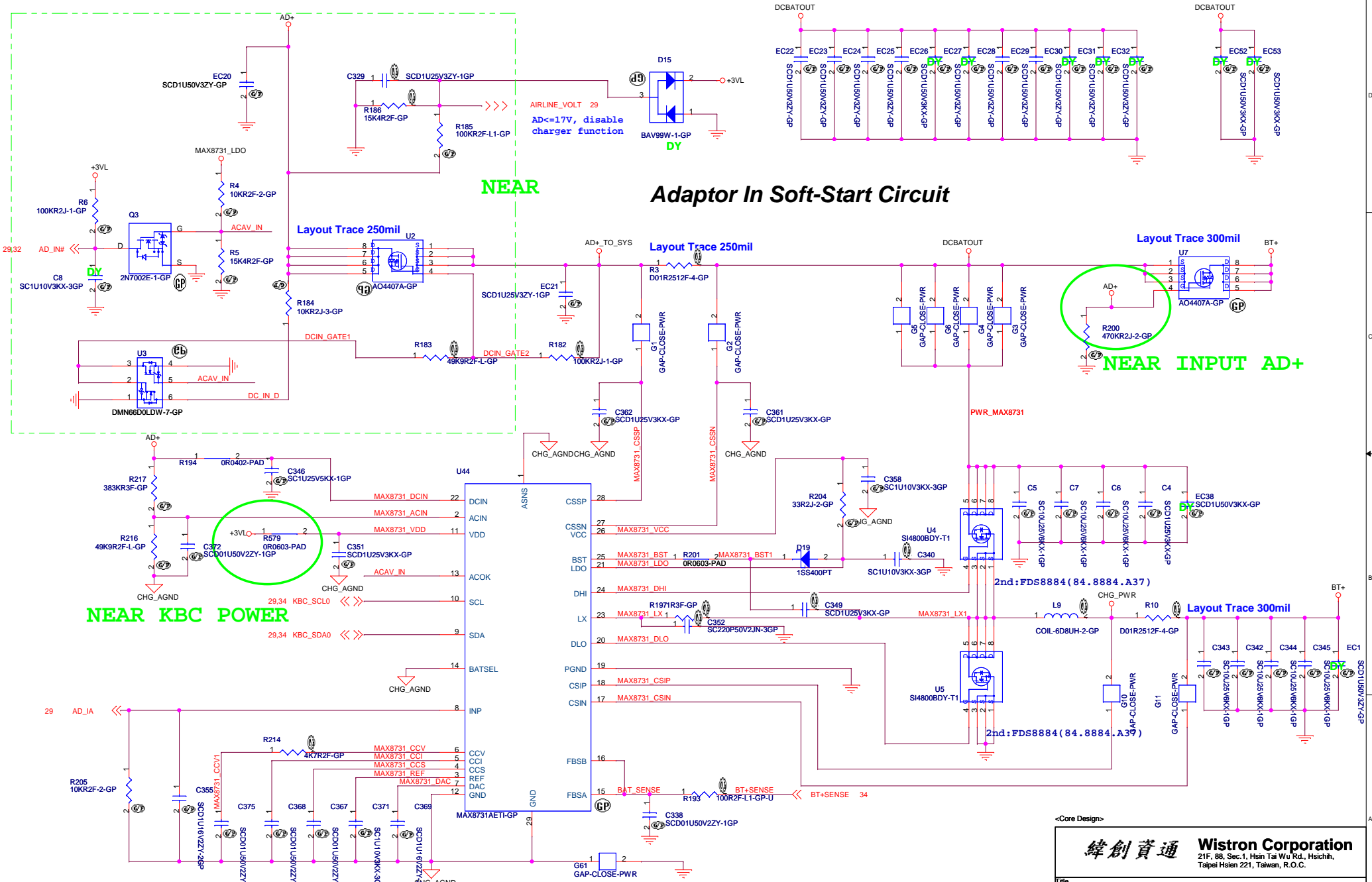
<Core Design>

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Title: **PWRPLANE**

Size: 43 Document Number: **HBU16 1.2** Rev: **1**

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Adaptor In Soft-Start Circuit

NEAR

NEAR INPUT AD+

NEAR KBC POWER

Need Check MAXIM Sming Use MAX8731 or MAX8731A

<Core Design>

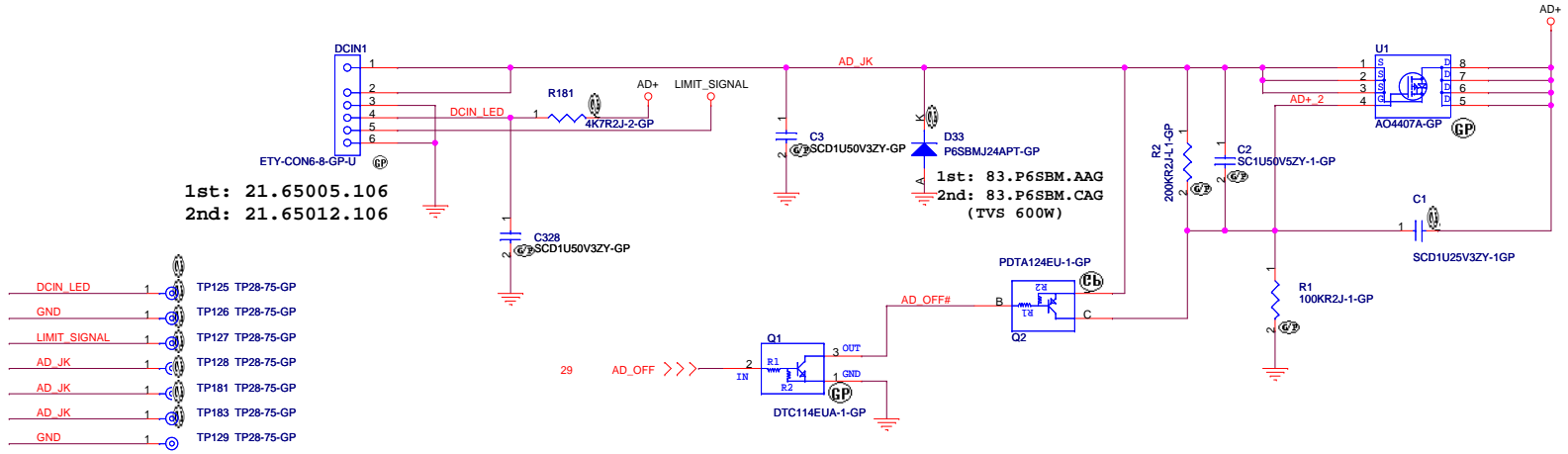
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8731ETI**

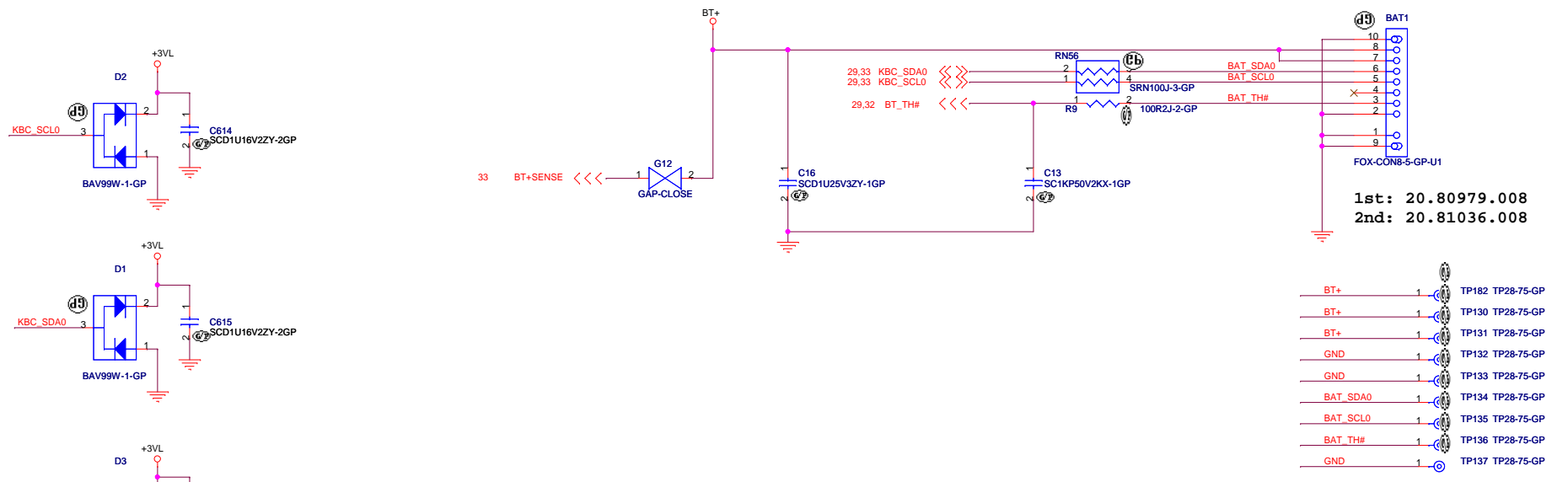
Size: A3 Document Number: **Warrior** Rev: **1**

Date: Thursday, July 09, 2009 Sheet: 33 of 41

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



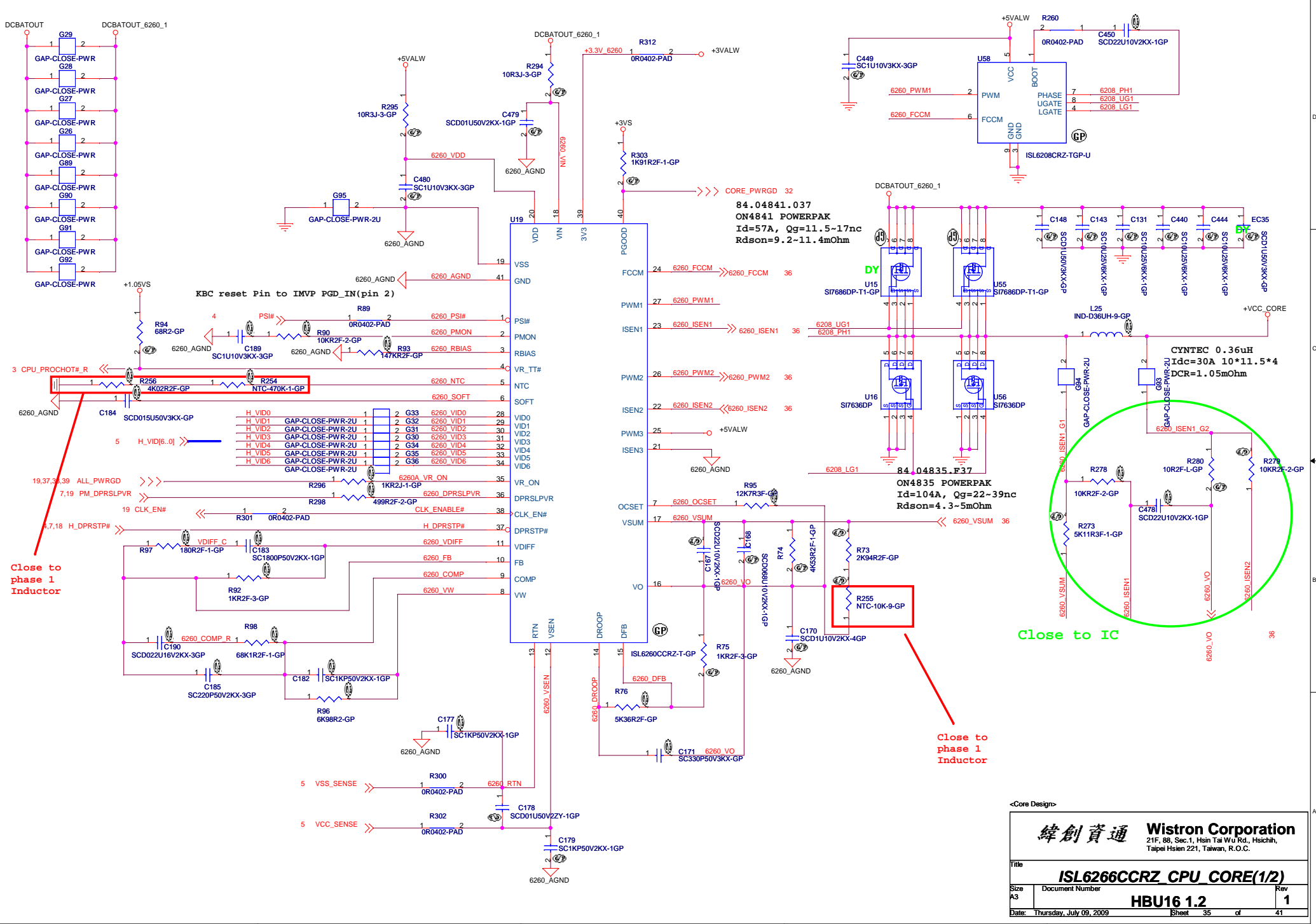
<Core Design>

緯創資通 Wistron Corporation
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Title: **AD/BATT CONN**

Size: A3 Document Number: **Warrior** Rev: **1**

Date: Thursday, July 09, 2009 Sheet 34 of 41



Close to phase 1 Inductor

Close to IC

Close to phase 1 Inductor

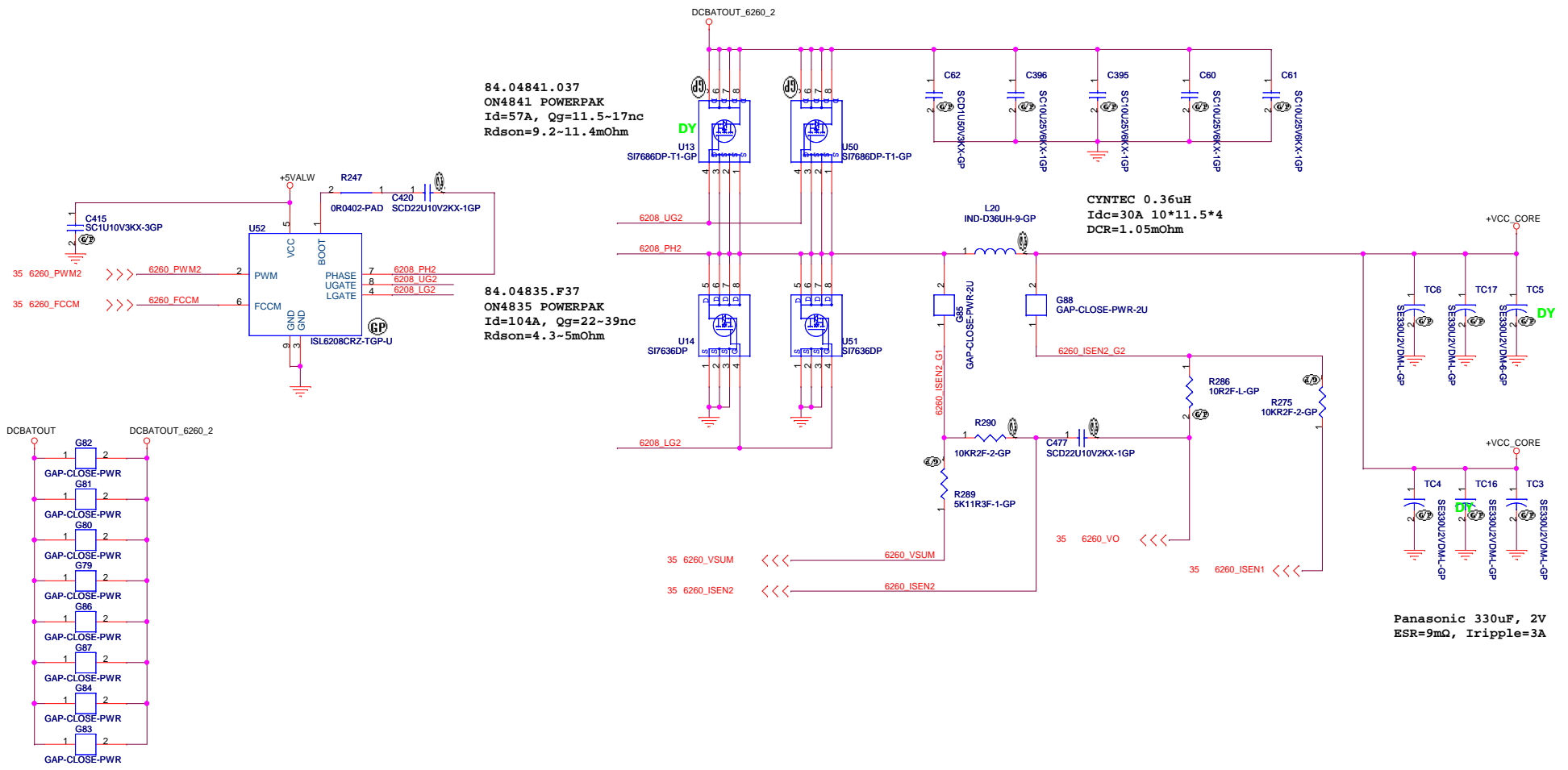
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6266CCRZ CPU CORE(1/2)**

Size A3	Document Number	Rev
	HBU16 1.2	1

Date: Thursday, July 09, 2009 Sheet 35 of 41

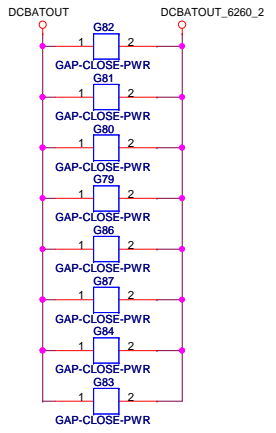


84.04841.037
 ON4841 POWERPAK
 Id=57A, Qg=11.5~17nc
 Rdson=9.2~11.4mOhm

84.04835.F37
 ON4835 POWERPAK
 Id=104A, Qg=22~39nc
 Rdson=4.3~5mOhm

CYNTREC 0.36uH
 Idc=30A 10*11.5*4
 DCR=1.05mOhm

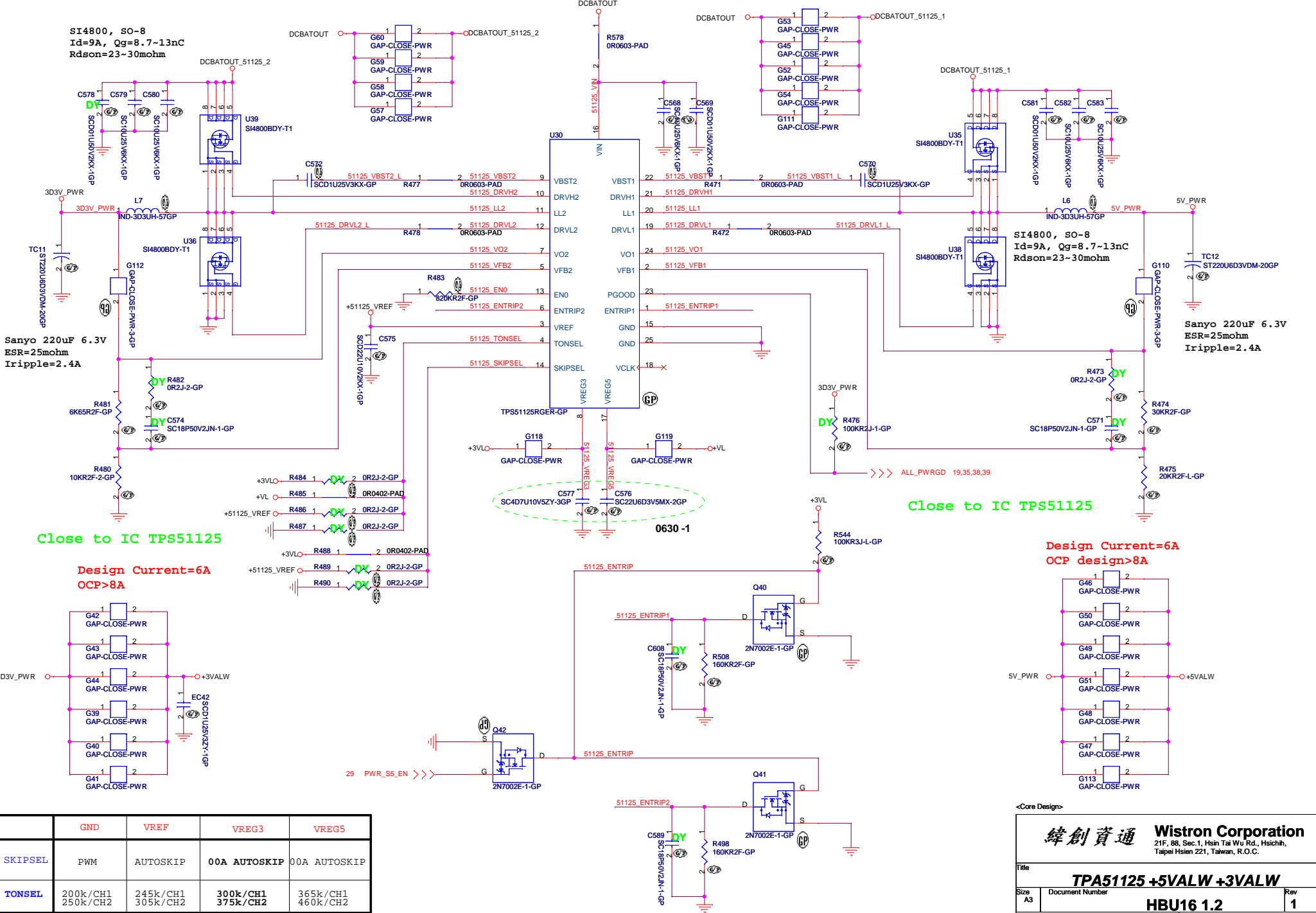
Panasonic 330uF, 2V
 ESR=9mΩ, Iripple=3A



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ISL6260CCRZ CPU CORE(2/2)	
Size A3	Document Number HBU16 1.2
Date: Thursday, July 09, 2009	Sheet 36 of 41

SI4800, SO-8
 Id=9A, Qg=8.7-13nC
 Rds(on)=23-30mohm



Close to IC TPS51125

Design Current=6A
 OCP>8A

Close to IC TPS51125

Design Current=6A
 OCP design>8A

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

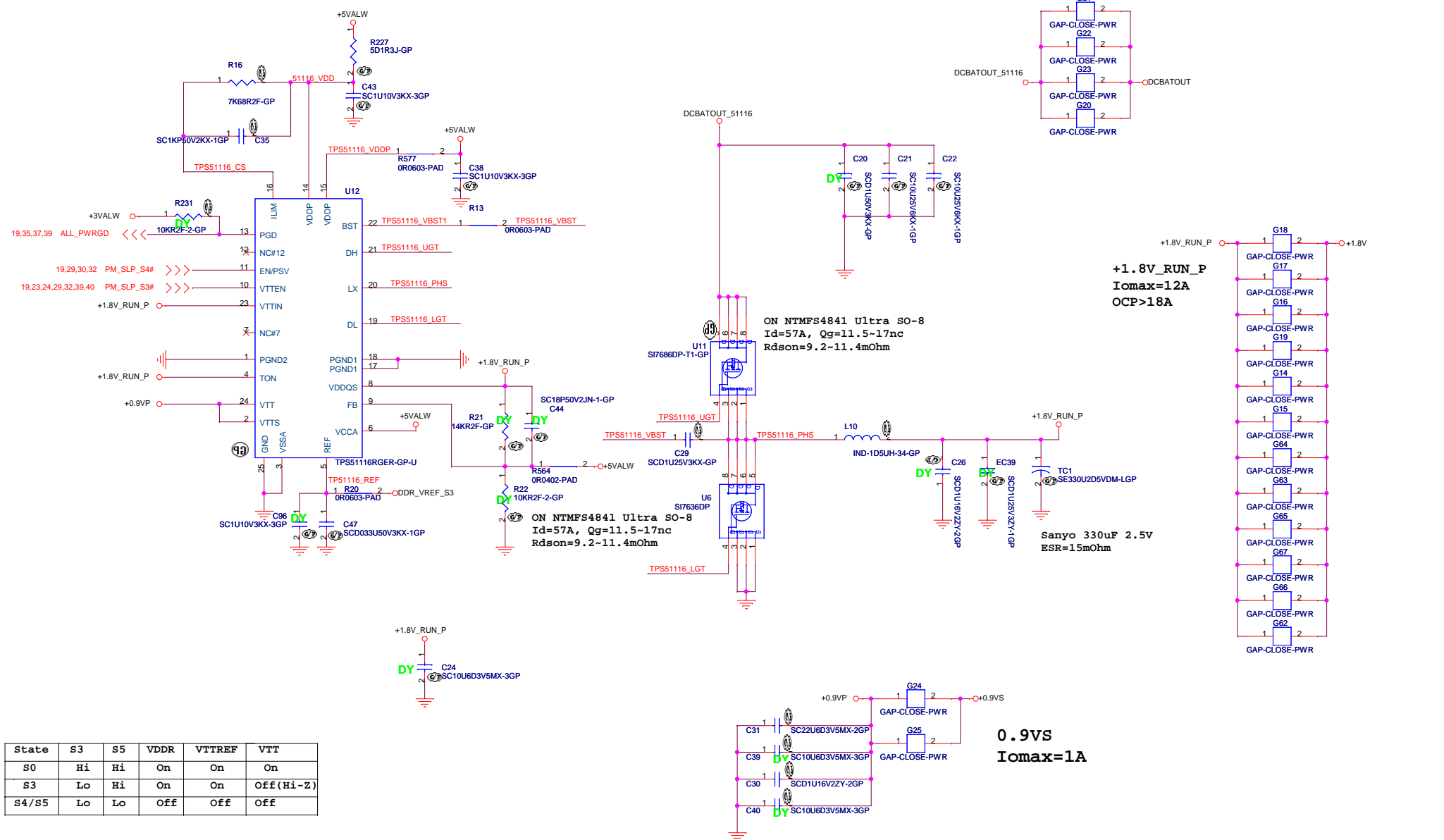
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPA51125 +5VALW +3VALW**

Size A3 Document Number **HBU16.1.2** Rev **1**

Date: Thursday, July 09, 2009 Sheet 37 of 41

TI TPS51116 for 1D8V and 0D9V



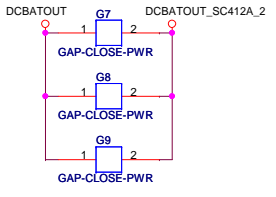
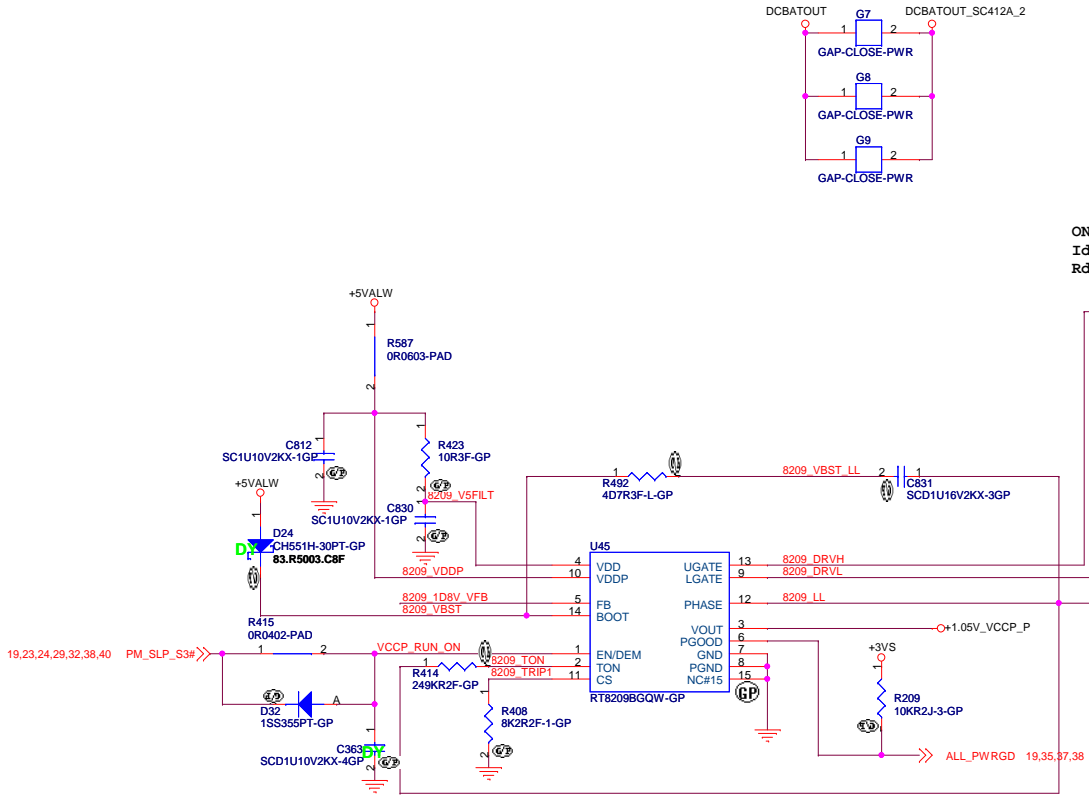
<Core Design>

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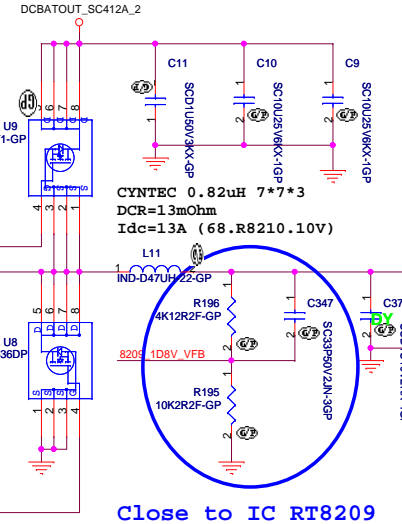
Title: **TPS51116 1D8V/0D9V**

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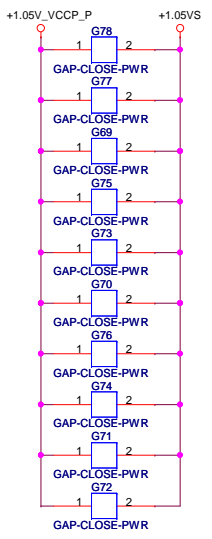
ON NTMPS4841 Ultra SO-8
 $I_d=57A$, $Q_g=11.5\sim 17nc$
 $R_{dson}=9.2\sim 11.4m\Omega$



+1.05V_VCCP
 $I_{omax}=15A$
 $OCP>20A$

Close to IC RT8209

77.C3371.13L NEC-TOKIN
 $330\mu F$ 2.5V 6m Ω
 $I_{ripple}=4.563A$

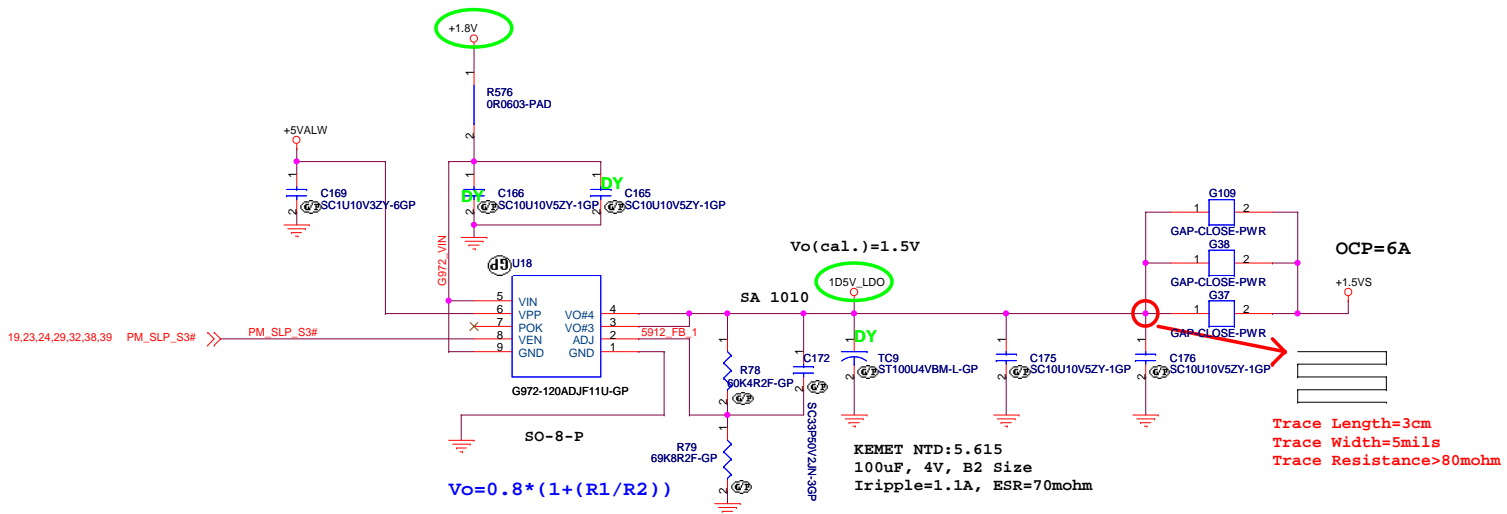


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 Taipei Hsien 221, Taiwan, R.O.C.

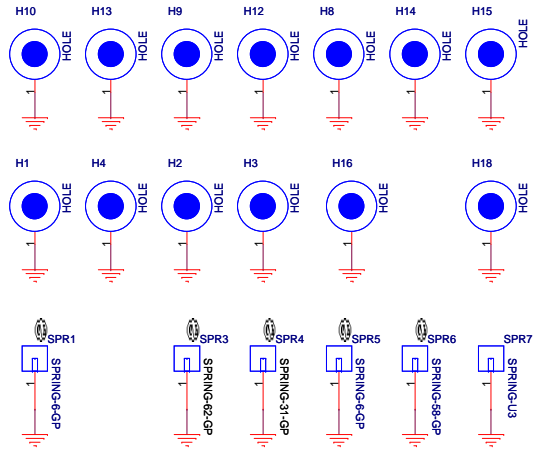
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Title			
GMT 1D5V LDO			
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- SPR1: 34.13B01.001,
- SPR3: 34.39S07.003, 34.39S07.101
- SPR4: 34.49U24.001,
- SPR5: 34.13B01.001,
- SPR6: 34.4B312.002, 34.4B312.101
- SPR7: 34.40U07.001, 34.40U07.101

